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Segmenting endoscopic images using adaptive progressive thresholding: a hardware perspective

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Abstract

Hardware realization of a novel technique based on adaptive progressive thresholding (APT) for the real-time segmentation of endoscopic images is presented. The APT algorithm is mapped onto a linear array of processing elements with each element of a particular segment communicating with its nearest neighbours. The efficiency and hardware portability of this technique justifies its use in applications that require high performance in real-time.

Keywords: Endoscopic images; Adaptive progressive thresholding; Segmentation

1. Introduction

The lumen region and boundary in intestinal images form the preliminary basis of the features used for navigation and guidance in an automated endoscopy system. The high speed and accurate extraction of these features is essential for real-time robotic navigation. Since the endoscope uses several light sources at its tip and the illuminating distances of these sources are limited, the intestinal surface lying near the light source will be brighter than the farther ones. Hence, the areas of lowest intensity represent the lumen region in an image. Several researchers have presented various methods to extract the lumen region from the endoscopic images [1,2]. An adaptive progressive thresholding (APT) technique for lumen extraction from a gray level endoscopic image is presented in this paper. Due to the excessive processing associated with image processing, many hardware implementation schemes for image processing have been presented in the literature [3,4]. A pipelined architecture for APT is proposed. The special purpose VLSI architecture uses an efficient encoding strategy to reduce the processing time as well as the communication time among the functional modules.

2. Adaptive progressive thresholding

Otsu's thresholding is based on a discriminant analysis that partitions the image into two classes G_0 and G_1 at gray level 't' such that $G_0 = \{0, 1,$

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$2,\ldots,t\}$ and $G_1 = \{t+1, t+2,\ldots,L-1\}$, where L is the total number of gray levels in the image. The optimum threshold t^* can be obtained by maximising the between-class variance. Repeated application of Otsu's technique adaptively in a systematic fashion leads to a more accurate thresholded value and this procedure is named APT. Recursive thresholding is continued till the Cumulative Limiting Factor (CLF) defined as the ratio of between-class variance and total variance in every Δth iteration becomes less than a predefined value. That is, the iterative procedure is stopped and the final threshold value is obtained whenever

$$\mathrm{CLF}(\Delta) < \alpha \frac{\mu_T}{\sigma_T^2}, \tag{1}$$

where α is a constant known as limiting parameter which can be trained using a number of images taken from a particular endoscopic camera. This takes into account the light intensity and distribution of the light sources mounted on the endoscope. The various computational steps involved in the APT algorithm are shown in Fig. 1.

3. Pipelined architecture for APT

The hardware architecture consists of a pipeline of cells, each cell capable of performing a well-defined function. The input–output operations occur only at the boundary cells. The pipelined architecture for APT based on a linear array model with only nearest neighbour interconnections is developed for an 8-bit gray level image of size 256×256. Some variations in the computational steps of the APT algorithm have been adopted to satisfy the area-time efficiency requirements. The first stage in the architecture is associated with intensity histogram (IH) and intensity (IA) area computations. The 64 Kbytes image data is stored in four 16 Kbytes RAMs (R_1–R_4) and the data reading process is multiplexed. The second stage of the architecture is to compute IH and IA accumulation. In order to facilitate this, both the IH and IA registers in the first stage are circularly coupled so that the content of each register can be transferred to its nearest neighbour after every circular shift operation. The IH accumulation (IHA) and IA accumulation (IAA) are performed by successive addition and accumulating the sums in the ACC registers in each circular shift operation. The between-class variance σ_B^2 is computed by successive multiplication. The σ_B^2 values are then passed to a maximisation circuit to obtain $\sigma^2_{B_{max}}|_i$. Similarly 16 parallel blocks perform their computations simultaneously in a pipelined fashion for the computation of $\sigma^2_{B_{max}}|_i$ for $i = 1,\ldots,16$. The register arrays holding the contents of 16 different values of the $\sigma^2_{B_{max}}|_i$ for $i = 1,2,\ldots,16$ and the corresponding t^* are then circularly shifted to enable the computation of the maximum value $\sigma^2_{B_{max}}$. If the maximum value obtained is greater than $\alpha\mu_T$, the progressive threshold operation is activated and the threshold t_i^* obtained is used as the top value of the IHA and IAA. If the new σ_B^2 satisfies the stipulated condition, the optimum threshold is obtained.

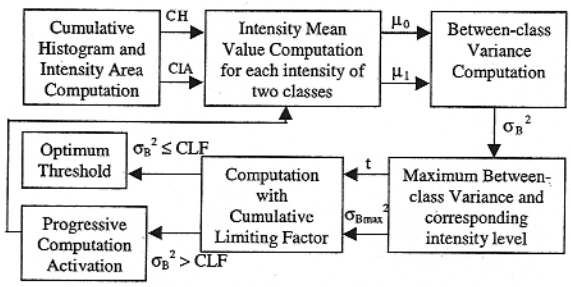
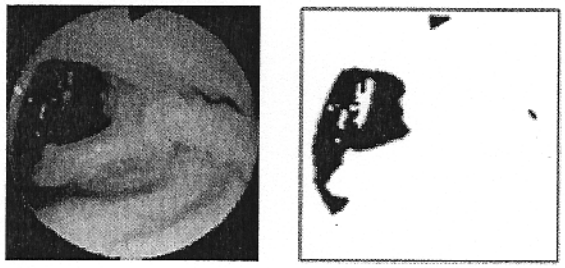


Fig. 1. Computational steps in APT.

4. Results and discussion

The APT algorithm was tested using a large number of endoscopic images of size 256×256. 8-bit gray level images were generated from the original colour images and a filter of size 3×3 was used to smoothen the images. The APT technique produced better results, as it is independent of the absolute gray level of the pixels contained in the darkest region. The optimum value of limiting parameter α was chosen using a training-set of images and was found to be 8.3 in our application.



(a) (b)

Fig. 2. Segmentation of a typical endoscopic image. (a) Original image (b) Thresholded image.

A typical endoscopic image and the corresponding thresholded image are shown in Figs. 2(a) and (b), respectively. Performance evaluations of the proposed hardware confirm that the overall time taken was about 0.16 ms for the same image. It is envisaged that an improved pipeline design with increased parallelism in deep sub-micron technology will significantly shorten the computation time.

5. Conclusion

An area-time efficient architecture for the real-time implementation of APT to segment endoscopic images has been proposed. Currently, on-chip memory core based VLSI design for an image of size 256×256 is being implemented for eventual fabrication using 0.35 μm CMOS technology. Further research work is in progress to develop a reconfigurable architecture by appropriate partitioning of various modules in the system.

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