

Design of an Efficient VLSI Architecture for Real-Time Correction of Barrel Distortion in Wide-Angle Camera Images

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Abstract – An efficient pipelined architecture for the real-time correction of barrel distortion in wide-angle camera images is presented in this paper. The distortion correction model is based on least-squares estimation to correct the non-linear distortion in images. The model parameters include the expanded/corrected image size, the back mapping coefficients, distortion centre and corrected centre. The CORDIC based hardware design is suitable for an input image size of 200×200 pixels and is pipelined to operate at a clock frequency of 50 MHz. The VLSI system will facilitate the use of a dedicated hardware that could be mounted along with the camera unit.

1 Introduction

Electronic video-endoscopy has become one of the commonly accepted forms of diagnostic and therapeutic procedures in today's medical practice. Video-endoscopes facilitate observation, documentation and electrical manipulation of the images of internal structure of the gastrointestinal tract. Equipped with wide viewing angle lens (fish-eye lens), cameras in these endoscopes can capture a larger field in a single image [1]. However, the images captured by these cameras also show barrel type spatial distortion due to wide-angle configuration of the camera lens. Barrel distortion shows non-linear changes in the outer areas of the image. For clinical Endoscopy where estimation of parameters such as areas and perimeters is critical, the distortion in images could cause significant errors [2-3]. Several researchers have proposed various mathematical models of image distortion and techniques to find the model parameters to correct the distortion [4-9]. In this paper, a dedicated pipelined architecture is presented to correct the barrel distortion in real time. The distortion correction technique implemented in this architecture is based on the least square estimation method presented in [10].

2 Distortion Correction Algorithm

The method to correct distorted images presented in this paper assumes that the distortion is purely radial about the distortion centre [10]. The idea is to map every pixel in the distorted image to an expanded/corrected image, and then to fill in all vacant pixels in the corrected image with appropriate intensities. Let (u_c', v_c') represents the distortion centre in the distorted image space (DIS), and (u_c, v_c) represents the corrected centre in the corrected image space (CIS). In DIS, magnitude ρ' and the angle θ' created by ρ' and the horizontal axis of a vector $\mathbf{P}'$ from the distortion centre (u_c', v_c') to any pixel location (u', v') are given by:

$$\rho' = \sqrt{(u' - u_c')^2 + (v' - v_c')^2} \quad \theta' = \arctan\left(\frac{v' - v_c'}{u' - u_c'}\right) \quad (1)$$

The same pixel can be assigned to a new location (u, v) in the CIS with the corresponding magnitude ρ and angle θ given by:

$$\rho = \sqrt{(u - u_c)^2 + (v - v_c)^2} \quad \theta = \arctan\left(\frac{v - v_c}{u - u_c}\right) \quad (2)$$

The mathematical relation between magnitude ρ' and ρ is defined with an expansion polynomial of degree N as:

$$\rho = \sum_{n=1}^N a_n \rho'^n \quad (3)$$

where a_n 's are the expansion coefficients that can be obtained using the least squares estimation technique [10]. Since the distortion is assumed to be radial about the distortion centre, the angles θ' and θ are the same. The location (u, v) of the pixel in the CIS can be obtained by:

$$u = u_c + \rho \cos \theta' \quad v = v_c + \rho \sin \theta' \quad (4)$$

2.1 Back Mapping

For any pixel in CIS whose intensity needs to be computed, it must be mapped back onto the DIS to find corresponding location (x', y') . The back mapping process can be described by a back-mapping polynomial of degree N as:

$$\rho' = \sum_{n=1}^N b_n \rho^n \quad \theta' = \theta \quad (5)$$

where b_n 's are the back-mapping coefficients that are calculated by using non-linear regression analysis employing least squares estimation for a finite number of points in the distorted image [11]. Then, the pixel location (x', y') can be obtained as:

$$x' = u_c' + \rho' \cos \theta' \quad y' = v_c' + \rho' \sin \theta' \quad (6)$$

2.2 Linear Interpolation

In most cases, the position (x', y') of the pixel calculated using back mapping method described in section 2.1 are non-integers; therefore, the intensity of the pixel is computed by linear interpolation of the four neighbouring pixels in DIS. Let A and B represent the integer parts of x' and y' respectively as denoted in Eq. (7a) where symbol $\lfloor p \rfloor$ represents the lower bound integer of the real number p .

$$A = \lfloor x' \rfloor \quad B = \lfloor y' \rfloor \quad (7a)$$

and the fractional parts of the coordinate values are represented as A' and B' .

$$A' = x' - A \quad B' = y' - B \quad (7b)$$

The four neighbouring pixels are (A, B), (A+1, B), (A, B+1) and (A+1, B+1) as illustrated in Fig. 1.

A	A+1
B	B
A	A+1
B+1	B+1

Figure 1: Pixel locations for linear interpolation

The linear interpolation of the intensities of the four pixels is performed as:

$$I'_1 = I'(A, B) \times (1 - A') \times (1 - B') \quad (8a)$$

$$I'_2 = I'(A + 1, B) \times (A') \times (1 - B') \quad (8b)$$

$$I'_3 = I'(A, B + 1) \times (1 - A') \times (B') \quad (8c)$$

$$I'_4 = I'(A + 1, B + 1) \times (A') \times (B') \quad (8d)$$

Then, the intensity $I(u, v)$ for the pixel at location (u, v) in CIS can be obtained by:

$$I(u, v) = \sum_{j=1}^4 I'_j \quad (9)$$

3 Distortion Correction Architecture

The design of the distortion correction architecture assumes the presence of the size of the corrected image, N back-mapping coefficients (b_n 's), distortion centre (u_c', v_c'), and corrected centre (u, v) . The design focuses on the process of back-mapping the pixels from CIS onto DIS, and computing the intensities for the pixels. Fig. 2 shows the block diagram consisting the four main modules of the architecture. Since the architecture is designed for a real time application, which requires fast computations of all the mathematical equations presented in section 2, all modules are designed by absolute pipelining of all the operations involved in these computations.

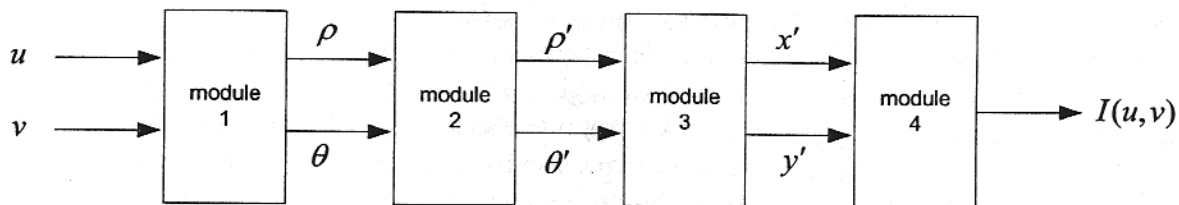


Figure 2: Block diagram of the distortion correction architecture

3.1. Module 1: Cartesian to Polar Coordinate Transformation

In order to back-map any pixel using the back-mapping polynomial in Eq. (5), magnitude ρ and angle θ representing the vector $\mathbf{P}$ from the location (u, v) of the pixel to the corrected centre (u_c, v_c) in CIS must be obtained. From the given information about the location of the pixel and the

corrected centre, the magnitude ρ and angle θ can be obtained by performing the Cartesian to Polar coordinate transformation. An unrolled pipelined CORDIC module is designed and implemented for this specific task. The CORDIC algorithm is selected to implement this because it can perform the transformation fast enough with a series of shift and add operations [12]. Fig. 3 shows the architecture of the pipelined CORDIC module with M iterations. By appropriately selecting the mode of the CORDIC algorithm, vector mode in this case, the magnitude ρ and angle θ can be obtained.

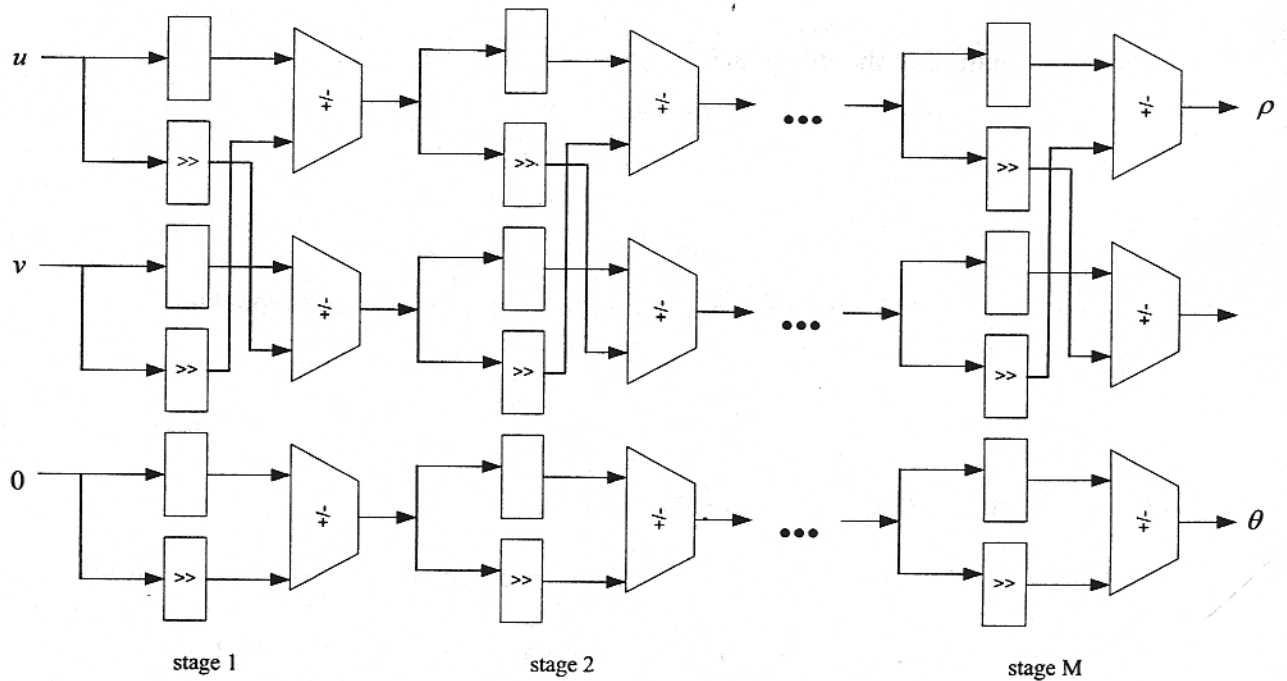


Fig. 3: Module 1- Pipelined CORDIC architecture

3.2. Module 2: Back-Mapping

Once ρ and θ are computed from the previous CORDIC module, ρ is mapped back onto the DIS to obtain ρ' based on Eq. (5), and the angle θ remains unchanged. The back-mapping coefficients are pre-computed and are stored in specific registers to enable their access at different stages of the pipeline. For this design, four back mapping coefficients are used. The only input for this module is ρ , and θ from module 1 is bypassed to module 3 for further Polar to Cartesian coordinate conversion. Fig. 4 shows the architecture for the back-mapping module where a pipelined multiplier takes 5 cycles to complete the multiplication and an adder takes 1 cycle. 'D' represents 5 delay stages to synchronize data from the adder with the data from the multiplier.

3.3. Module 3: Polar to Cartesian Coordinate Transformation

Once magnitude ρ' and angle θ' are available from the back-mapping module and module 1 respectively, they can be used to determine the location (x', y') in DIS by performing the Polar to Cartesian coordinate conversion. Again, CORDIC algorithm is employed for this purpose. The

pipelined architecture implemented in this module is similar to that of module 1 shown in Fig. 3. In this case, by selecting the rotation mode of the CORDIC module, the x-coordinate and y-coordinate values of the location (x', y') are obtained for every radius ρ' and angle θ' .

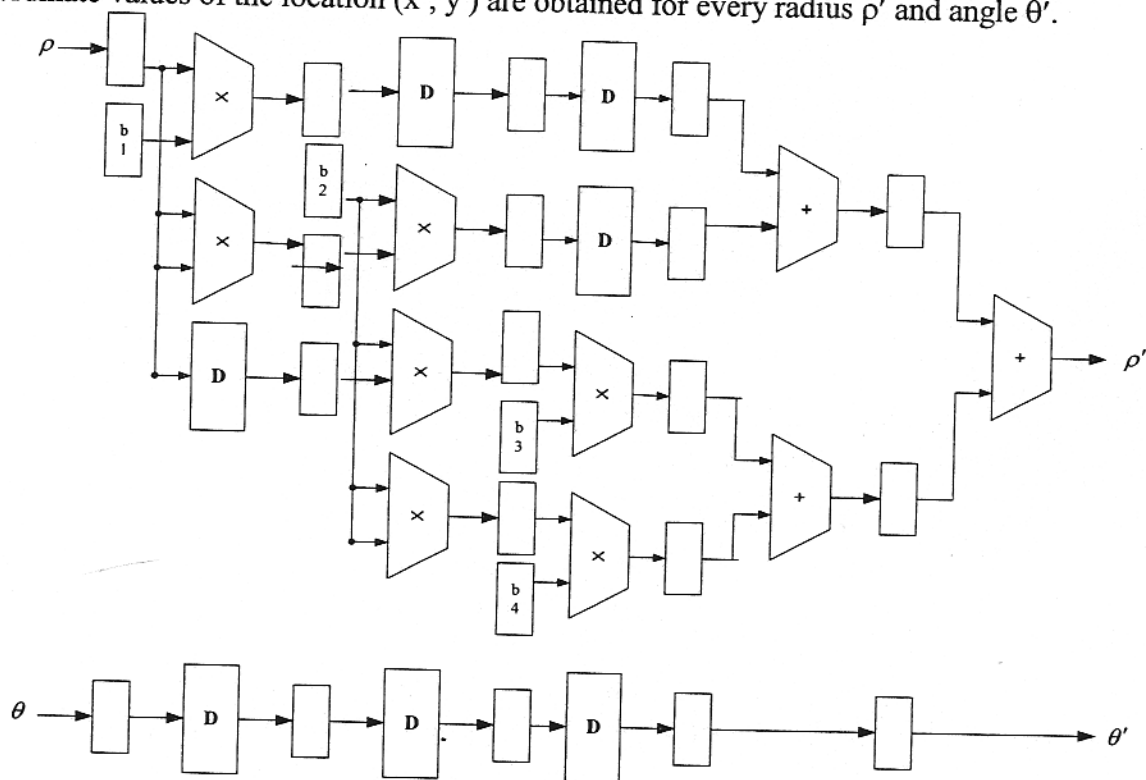


Fig. 4: Module 2 – Pipelined back mapping architecture

3.4. Module 4: Linear Interpolation

The design and implementation of the linear interpolation module is in progress. The purpose of this module is to determine the intensity of the pixel at (x', y') by using the intensity values of the four neighbouring pixels of (x', y') . Once the input coordinates (x', y') is available from module 3, this module communicates with external RAM where the distorted image pixels are stored and acquires the intensity values of the four neighbouring pixels, and it then performs the linear interpolation process as discussed in section 2.2.

4 Results and Evaluation

The first three modules - two coordinate transformation modules and the back-mapping module - have been designed and built with Altera's Quartus II design software. The pixel locations and intensities are represented with 24 bit registers in the architecture. The two CORDIC modules, which are responsible for transforming the pixel coordinates occupies 3670 logic elements (LE) each in an Altera's APEX 20K device, and they are operating with a clock frequency of 50 MHz. The back-mapping module occupies 6090 logic elements by itself and it is also operating with a clock frequency of 50 MHz. The total latency for one pixel going through all three modules is

approximately 1.64 μ s when operating with 50 MHz clock. Since all modules in the architecture are pipelined, the distortion correction system would be able to continuously produce intensity value of a pixel in every clock cycle after the initial latency.

5 Conclusion

Pipelined design of an efficient VLSI architecture for real-time correction of non-linear distortion in wide-angle camera images has been presented in this paper. The architecture is designed based on the method of back-mapping the pixel and performing the linear interpolation of four neighboring pixel intensities. The back-mapping coefficients are obtained by least squares estimation technique. All functional modules in the architecture are pipelined to satisfy the speed in correcting distorted images for real time application such as in video endoscopy. Three modules have been designed and simulated in Altera's Quartus II software, and the results are satisfactory. The implementation of the final module, which calculates the intensity of a pixel with linear interpolation of the neighboring pixels, is in progress.

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