<Jones, Richard> Ok

<Jones, Richard> How's everyone doing on the labs thus far.

<Jones, Richard> Lets start with lab 1.

<Jones, Richard> Anyone out there who hasn't shipped theirs yet?

<Tharpe, Dennis> I will ship mine this weekend

<Jones, Richard> John and Judd, have yours been shipped?

<Fallon, John> I gave mine to you last monday

<Lentz, Judd> Lab one is going well but I need finish up

<Jones, Richard> Can I help you?

<Lentz, Judd> lab 1 and 2 finished this weekend.

<Jones, Richard> Ok. Any questions on Lab 2?

<Lentz, Judd> no I think I have it work has just been very tasking

<Lentz, Judd> lab 2 good

<Jones, Richard> John, I understand you have a lab 2 question?

<Fallon, John> I think I figured out my problem

<Lentz, Judd> just got proto board in from preist yesterday b 4 class

<Fallon, John> I didn't have the clock on 5% duty cycle

<Jones, Richard> That would do it.

<Lentz, Judd> Hope to catch up totally this weekend

<Fallon, John> I couldn't get my high output on the monostable to stop being high

<Jones, Richard> Remember that both RELTOR and the TWO time steps should be at 1e-4.

Also for the monostable, don’t use the calculated value for R. Use something in the 10k range. Any more questions about lab#3?

<Jones, Richard> The CMOS driver is only for the project.

<Jones, Richard> Use the TTL driver for the lab.

<Jones, Richard> Look at the parts list on the lab.

<Jones, Richard> I now have my version 6.11 MultiSim.

<Jones, Richard> I note that the virtual o-scope now has an invert button for channel B.

<Jones, Richard> It's getting closer and closer to being able to simulate all but the actual LCD.

<Wilson, Dan> I have Netmeeting Ver 2.1 followed by (4.3.2203)

<Jones, Richard> Lab 4 and Lab 5 have been posted.

<Jones, Richard> Hope everyone has had a chance to read thru lab 4.

<Jones, Richard> The first circuit is a simple Ripple counter.

<Jones, Richard> Dan, your netmeeting is not the one I have on my home page for download.

<Jones, Richard> That's why you don’t have audio.

<Wilson, Dan> I'll have to redo it then

<Jones, Richard> Should be version 2.11, build 432519

<Lentz, Judd> I had the same trouble until I went to find and deleted all netmeeting stuff then reinstalled

<Jones, Richard> Make sure that you deinstall the one you have, install the new one. Reinstall the Meeting tools, then run the utilities.

<Wilson, Dan> Do I uninstall first then instal or does it matter

<Jones, Richard> You must deinstall first.
Make sure that you put the Vcc and the digital ground in the circuit first.
Feel free to use the Vcc within the circuit where needed.
Don't use the digital ground for anything but to have it sit there and look pretty.
Everyone who has the latest version and build of netmmitting has audio.
Those who don't, don't
That doesn't help me at all.
Read last week's chat session.
Now, make sure that you don't connect a wire any closer than two grid lines from an existing wire or junction. Label the wires as shown.
This circuit WILL NOT WORK without the RELTOR and TIMESTEP changes.
Mr J, I'm going to go get this netmmitting issue fixed...
Great, feel free to call me on it.
Hook up the logic analyzer and observe the four outputs in relation with the clock input.
(not shown in picture)
Professor, I can't see my grid dots anymore - even when checked off on list.
Answer the questions carefully.
Don't skip any.
Dennis, go to the Pull down menu, VIEW/GRID VISIBLE.
I have one more question on lab 2. For the bypass diode circuit figure 6, should we use the ideal diode.
You can, but I would prefer a 4001 series.
ok
General purpose.
I believe it is in the schematic.
and just how close is close to 1kHz
Back to lab 4, part 1.
I keep getting 1.5 or so
1.5 what?
kHz
Then modify your C and R choices.
Tried view grid visible and it didn't work
Make sure you are using C1 in your calcs and not C.
OK
Dennis, most likely your computer needs to be rebooted. Memory issue.
OK
If it's been awhile since you downloaded lab 2, there is another revision there. You are not required to use it but it might help you with your calcs.
There a frequency equation which might help on this question.
Any more on lab 2?
Can I go back to lab 4?
Are there any questions on how the Word Generator is programmed for part 1?

PART 2

Just noticed that Figure 3 is messed up.

Not really needed as long as Figure 2 is ok.

Should be self explanatory.

You have graduated to where you are going to write the Generator programs yourself. Use the bit sequence given with PO being the LSB or BIT 0. Any questions?

So MR goes to the 0 on the word generator?

No, sorry, right most bit is P0 which is bit 0.  MR is bit 7.

Ok got it.

MAKE SURE YOU DO.

I will grade as if you do.

Page 4 of 9.

You need to observe the output closely and observe how TC’ works in relation to the other outputs and the clock. If you need help, feel free to go to TI or Motorolas home pages and read the spec sheets on this chip.

The signals are always discussed in the specs.

This lab has you doing a lot of reprogramming.

There are a LOT OF GRAPHS to prepare, include, and discuss in your report.

bless you

Feel free to learn how to use the properties Cut and Paste in the grapher.

Saves a lot of time.

For some reason Figure 5 is messed up to.  I’ll fix these two over the weekend and post a rev.

With this counter I’m interested in MIN/MAX and the RIPPLE CLOCK outputs.  Again, a little research might back up what you observe.

Since the lab requires you to download and include the specs anyway, might as well do it early.  You don't have to use Motorola.  Go to any company that you can find the specs for the chip.

Make sure that you read the state machine design paper.

It will be finalized this weekend.

YOU MUST HAVE STUDIED THIS BIG TIME before you attempt lab 6.

I would take it as a personal favor if you could critique the labs via email.

I put a lot of time in on these and I want to make them as good and permanent as possible.

When are we to begin our journals and weekly email progress reports?

You start the journals and progress reports with the project.

As always, I'm available by phone and email if you need help.

I have nothing further mind if I go and work on lab2 more now

No problem John.

NO CLASS SAT.

Has everyone turned in lab # 1 ?
Almost everyone. I'm missing 2 of you. possibly 3. I inventory this week. Can't grade them until I get them all. So how long do we have? Remember to copy everything before you send them to me. You need to finish and ship lab 1 by sat. something happened to my sound Lab 2 by Wed. I may have missed it but is there a good explanation of what the i/p's to the function generator Lab3 by next sat if possible. We need to get caught up. I in put What do you mean? i mean function analizer from later part of lab 1 Functionb analyzer. OK. what about the function analyaer. strike last wait one you are making me homesick with this navy talk! the input connectons to the logic analizer still fresh in my mind only out a year The only ones you will use are the inputs along the left side. We will contentue to use the internal clock. Have you used it at all yet? yes but when it graphs out I was confused by some of the plots for the d flip flop part of the lab