This Chat session is a combination of both the Thursday and the Saturday Chat sessions. I took the best of both to make this one document. In addition, it has the graphics used in the Saturday session vice the rough sketches used in the Thursday session.

Thursday attendance:  Brady, Gibert, Jason Jones, Khol, Satterfield, Dick Wilson, Bingham (6:15), Prokopuk (6:40)
Saturday attendance:  Bledsoe, Prichett, Seriani, Baldwin (1:28)

AUDIO NOT WORKING:
<Jones, Richard> Baldwin, can you hear me?
<Baldwin, Richard> No.
<Jones, Richard> Did you run the NetMeeting Tuning Wizard before coming on-line today?
<Baldwin, Richard> I had audio working last weekend after the last meeting, but it isn’t today. I ran the Tuning Wizard when I re-installed NetMeeting last week.
<Jones, Richard> You guys need to get in the habit of running the Tuning Wizard just before signing on each week. This way your connections get tested. It is always possible that you have your mike and headphones plugged in reversed. Also, it is a good idea to bring your computer up from a cold start (i.e. turned off) just before you log-n to the class. There are a lot of applications that get hold of your sound driver and don’t return it when they are done. Starting from a cold boot usually fix that problem.

LAB #3 questions:
<Kohl, Kristopher> I do have a question about lab 3 though on the way I set my switches up. I realized through a lab I had with Williams, that you must tell the chip both ones and zeros. So I set up my switches like I have VCC to a 1kohm to the pin then connected to that node, I have my switch to ground. The way I have it set, is that I have a "1" with the switch open and "0" with the switch closed. That is the only way I figured out how to make it go 1 and 0 with one switch.

<Jones, Richard> Are we talking about the simulator or hardware? (ANS: HARDWARE)
<Jones, Richard> Are we talking a single throw double pole switch? (ANS:SPDP)
<Jones, Richard> Attach one end of the switch to ground, attach the other end to the pin in question. Also at the pin connect a 1 k ohm resistor from the pin to Vcc. This is a pull-up resistor. The size of the resistor is dependent on the max and min currents that the pin can sink.

<Jones, Richard> Just realized that the switch stuff was pulled from the Lab 1 write-up. Will post it separately. I go in big detail in lab on this for both the simulator and the hardware usages. I will find it and post it as a Lab 1 intro. It has a LOT OF GOOD USEFUL stuff that might come in handy for the project.
Lab #4 ITEM:
<Jones, Richard> Did everyone not in class on Tuesday what I said about the 4516 and not being able to count down. If I said to count down with the 4516, count up counting instead and comment on that problem as one of the bugs. But there is still a bug I want you to find with the chip counting UP.

STATE MACHINE TUTORIALS FOR DOWNLOAD.
<Jones, Richard> If you will note, there are two document links right below lab 5 on the course homepage. They are machine tutorial # 1 and # 2.
<Jones, Richard> If you see them on the page, HAND’s...... DOWN
<Jones, Richard> These two tutorials are to prepare you for lab 6. It is a MUST that you study and understand both of these before next Thursday. You might even want to simulate them.
<Jones, Richard> One of them is titled ”State Machine Design Example, Simplification by Observation.” **Do this one 1st.**
<Jones, Richard> It is a tried and true state machine design routine which ends up with a very simple circuit.
<Jones, Richard> The second one is titled “Overview of State Machines.” It is less simple then the 1" one but it does start out at a lower level. In addition, there "MIGHT" be a minor 1 bit error in one of the tables. Don't remember if I fixed it or even what it was.
<Jones, Richard> I say again, you won't survive lab 6 without this background. In addition, you will be getting a leg up with the course.

LAB #5 General
<Jones, Richard> The actual discussion today is very short on lab 5. Lab 5's purpose is to do two things. To understand phase shift management for your project and also, what you end up with in the lab will be useful for testing your project at home since you don't have access to my test platform for your project. By the way, I don't let my locals use the test platform either.

LAB #5 page 1
<Jones, Richard> Page 1 of the lab. The project platform consists of a wheel attached to a spade handle and an optical sensor. This sensor will output two phases one of which will always lag the other by 90 degrees. The phase relationship is related to the direction of the wheel. The number of pulses is related to the number of rotations of the wheel.
<Jones, Richard> Figure 1 shows that Phase b is lagging phase A by 90 degrees.
LAB #5 page 2 and 3: Read closely.
LAB #5 page 4

<Jones, Richard> Note on the circuit in Figure 2. Feel free to replace the 74LS04 inverter with a 74LS00 (NAND) with its inputs shorted. I like to use the simulator NAND gate model more than the simulator NOT gate model.

<Jones, Richard> Figure 2 is a multi-phase clock. The switch, S1, is found in the same parts bin as the resistors. You can change the control button to flip switch positions during simulation to any key from the space bar to A - Z. WARNING: make sure that you have not selected it on the sheet when running the simulation. It won’t change positions unless it is deselected!

<Jones, Richard> This circuit will output two phases which are out of phase by 90 degrees. It does this by turning the XOR into either a buffer (with one pin tied to ground) or an INVERTER (with one pin tied to Vcc)

<Jones, Richard> Make sure that you are using the scope in this lab, not the logic analyzer for this lab. The reason is that we need to be more realistic and be in the time domain for this lab. Make sure that we always have phase A in channel 1 and always trigger off of phase A, channel 1. This will keep you in a common frame of reference.

<Jones, Richard> My locals perform this lab in hardware vice simulation.

Question about the FIGURE 2 circuit troubleshooting:

<Seriani, Richard> Tried Fig 2 this morning could not get it to work on EWB 5.12. Can I call tomorrow if I can't fix? I couldn't get any output on either phase

<Jones, Richard> Before you email me the circuit, do the following:
<Jones, Richard> Go to edit and "select all", cut, close the circuit by selecting NEW page, paste the circuit where you want it, go back in and change the default settings to the e-4 settings and then test. It might help to delete the o-scope and put a new one in.

<Jones, Richard> (Turned out to be a Vcc connection to the PRE’s and CLR’s which wasn’t working. Deleted the Vcc and replaced it with a second one and it worked.)
Lab #5, page 5:

Page 5. Answer the questions. BEWARE, your answers won’t match mine if you aren’t triggering off of phase A, channel 1. In other words, you will be WRONG. When answering the questions on page 5, it is important that you follow the directions above Figure 2 on page 4. Make sure that you have the o-scope, either your virtual or a real one (if you choose to do this in hardware), is set to trigger on channel 1, phase A. This keeps the phase relationships predicable from my viewpoint.

Keep this circuit together because we are going to add to it on page 6.

Lab #5, page 6:

Page 6. We are going to add a D flip-flop to your circuit. Figure 3 is a 7474 D flip-flop. I haven’t tested this model in this version. You need to test it yourself. It didn't work right last version but it most likely will work in this version. Now, you can use the 7474 model in MultiSim but make sure it works. Do this separately by testing it before hooking it up to the circuit.

Lets note a couple of things about the 7474 D flip-flop. Seriani, what edge does it trigger off of?
Seriani, Rising.
Jones, Why?
Seriani, No inverting circle on input. Correct. We actually say "Leading vice rising."

This is important for two reasons. The first is that as I said, I haven’t tested this 7474 model in this version. As we noted with the 4516 chip, there are still some bugs in chips models. So, we need to know how to make a 7476 operate exactly like a 7474. Second reason. You will need to build into your project the ability to know the direction the wheel is going. The output of the D flipflop tells that direction. Now, if you happen to have an extra JK on your board because you used the second one on a chip for another purpose, why not use it instead of adding a 7474 chip to your chip real estate.

Jason, the 7476 that you used last lab. What edge did it trigger on?
Jones, Jason, falling
Jones, Richard, right. (We actually say “trailing edge”)
Jones, Richard, So, if your replace the 7474 with a 7476, we need to do something to make the 76 chip trigger on the leading edge vice the trailing edge.
Jones, Richard, Debbie, what do we do?
Bingham, Invert it
Jones, Richard, right. If you don’t remember how to turn a JK into a D flip-flop, go back and review the write-up in lab 1.
Figure 4 page 6. You are going to build a digital commutator and then observe the outputs on the o-scope, not the logic analyzer.

You could use the Logic Analyzer, but I don't want you to. You can use it to print out a Figure like Figure 4 for your report but I want you to practice with the scope. In order for you to have it look like mine, Phase A MUST lead Phase B as shown in the Figure. Make sure that you keep phase A in channel 1 and trigger off of channel 1 while you are measuring each of the commutator outputs.

Is the last AB in fig 4 not A and not B?

They are both not’d.

Yes. my printout is somewhat smudged

Again, feel free to replace the inverters in Figure 4 with NAND gates.

Note that at the top of the waveforms you see phase A and phase B. What I want to do set it up so that phase B is lagging phase A in the scope. Then I want you to leave Phase A in the scope, and replace phase b with each of the outputs in the order shown. As long as you keep triggering off of phase A, the observed phase relationships should match what you see in Figure 4.

Lab # 5 Formal Report

This is a formal report lab.

follow format instructions closely.

I'll get 1 and 2 shipped back next week, still waiting on the others.

PROJECT IN GENERAL: (have the Project handout in hand)

I am a company CEO trying to hire another company to build a prototype for me that can measure in curves as well as straight lines. I've put out a bid request for companies like yours to bid on building me a prototype.

The intro talks about what I want and who its for. I want the electronic portion of a digital tape measure prototyped by your company and sent in for testing. I'm not hiring your company to build a bunch of these, just 1! So when you do your cost estimate in the formal report, you can't spread the cost's over a bunch of the product. More on this later.

There are a lot of documents about the project, the reports, the journals and the parts to download, printout, and study for next weeks intro #2. Read the journal handouts and have questions next week.
PROJECT TEAMS:

Teams are not allowed. I don't allow locals in teams either, just haven't changed handout yet.

Your COMPANY name and position for the project:

Page 3. I want you to name your company and give yourself a position in it, i.e., head engineer, CEO, or just coffee gopher for all I care. All correspondence should be from your company from your POSITIONS viewpoint. Your formal report should have letterhead that you have designed for your company.

PROJECT ORAL REPORT

Even though the Project Document as currently posted mentions on, there isn’t one. Since you have to do one of these for your senior design project, I dropped the requirement.

PROJECT JOURNAL

You will need to keep a Design journal. There's a document on the site which discusses journal req'ts. Read before next week. NOTICE. The journal is a percentage of the grade but it is also PASS/FAIL. Every semester I flunk at least one student because he/she blew off the Journal req't. Read the req'ts closely!!!!

Can journal be more than one volume? if 1st book is not large enough?

VERY DEFINITELY. THAT'S THE RIGHT ATTITUDE!!!

THE PROJECT DESIGN PROCESS (THURSDAY)

You will begin your design on a breadboard. You should completely get it working on the breadboard before you even consider shifting to the wire-wrap stage. Then you should transfer it one stage at a time starting with the LCD and its drivers to the wire wrap board. Get each stage working in wire-wrap by it self. Then connect with the remainder of the circuit on the breadboard and get that working. Don't move a second stage to wire-wrap until the earlier stages are working. Then move the next stage to wire-wrap. Get it working by itself. Then wire wrap it up with the previous stages already on the board and get them working. Then connect with the stages left on the breadboard and get them working.

Repeat until you have completely moved everything except for the phase test circuit to wire wrap. Students who take this construction method, usually get their circuit working. Those who try to wire wrap the whole thing up at once don't!!@!!!!!
THE PROJECT DESIGN PROCESS (SATURDAY)

<Jones, Richard> Once you have the project working on the breadboard, successful students do the following: (failing students ignore me on this one)

<Jones, Richard> Starting with the LCD and its drivers, transfer to the wire wrap board and wire wrap (WIRE-WRAP is discussed during lab 7 project intro discussion)

<Jones, Richard> Once you have carefully wire-wrapped it, connect it to your working circuit on your breadboard and test it. Don't try to transfer the entire circuit at once. Yes I'm yelling here. Wire wrap is a rats nest from hell type of system. It is murder to troubleshoot. Don't move more chips thus more wraps until what you have already wrapped has been tested. Once the driver and LCD stage is complete, transfer the counter stage, test it by itself on the wire wrap board, then connect it to the rest of the circuit on the ww board and test again. Once that passes the test, connect to what’s left on the breadboard and test again. Repeat this process until the entire circuit is wire wrapped and tested on the ww board.

PROJECT WEEKLY EMAIL UPDATES

<Prokopuk, > Are the weekly e-mails due starting after lab #7?

<Jones, Richard> Yes, I should get the 1st update by the following Saturday after the lab starts. My weeks go from Monday to Sunday.

<Jones, Richard> I expect a email progress report, written from your company viewpoint weekly. I will not read it if the subject line is not in the given format. If help is needed, put HELP as last word of subject as shown in the write-up. Make sure you give me contact info.

<Jones, Richard> These e-mails are part of your grade and the grade will go down if I don't get one. Paste copies of these e-mails, cut to size, in your journal at the correct date locations.

<Seriani, Richard> Does email need letterhead on it?

<Jones, Richard> No. The letterhead is for the formal report.

<Prichett, James> Is there a limit as to how long you desire the Email to be?

<Jones, Richard> As long as needed to A: tell me what your progress is, B: any problems met and defeated, C: goals for next week D: any help requested.

<Jones, Richard> Don't run off at the mouth. I'm a very busy CEO!

<Seriani, Richard> Would you like email in bullet format or complete paragraphs?

<Jones, Richard> Bullet would be great, normally get a combination of bullet and para.

<Jones, Richard> James, question?

<prichett, james> Do we have any submittal’s before the weekly progress reports begin?

<Jones, Richard> No. The 1st weekly email is due the week after lab 7 session.
SPECS - The 4543 driver

You are required to use the 4543 driver. No substitutions. This is a good thing. The driver has a blanking input for the leading zero spec. and it has the xor gates from lab 3 built into it. It’s a CMOS chip but is fairly TTL compatible. But, since it is CMOS, you might be wise to order 6 vice 3 just in case.

SPECS – The MOD Counter

As pointed out earlier, the optical encoder will output two phases of pulses based on the rotation of the wheel and its direction of rotation. Using the numbers of pulses/rotation and the diameter of the wheel, you will calculate the number of pulses/inch. Knowing this, you will build a MOD counter, Lab 7, to count the pulses and output a pulse after every inch. The hardest part of the design last semester was the mod counter (lab 7).

SPECS – The Reset Button

Switch: reset, must reset all necessary counters to zero. This button is the only place where you are allowed to solder in the project. Beware! A lot of students tie there reset switch to the master resets/ “pl” pins on all of their chips at the same time.

Seriani, can you think of any problems with this?

I don't know the answer.

Any one out there want to hazzard a guess? Hint: specs sheets give some specs about input and output pins.

Does the word "current" bring anything to mind?

Fan out?

You’ve got the right idea. The power supply will only be providing a certain amount of current. If we divide that at the button between all the chips which have pins to be driven, some of the chips will not get the needed current, therefore they won't work.

Now, you might not notice at home because your supply might provide enough current to go around. But the specs tell what I provide, and I purposely don't provide enough! God I'm an “ a---hole”

Any idea how to fix this?

Buffers?

Good job. Give the man a gold medal.

A buffer can spread the fan in around. One way to get a cheap buffer is two use an OR or an AND with the inputs shorted together.

That’s as far as I go on this one.
SPECS – The Logic Family

Required Logic Family type. This paragraph will change to the following: Must be TTL compatible. Can be LS, HC, HCT, or F. Whatever you choose, it must either be TTL compatible or you must use techniques to insure compatibility.

SPECS - Leading Zero

Look at the following numbers: 001, 050, 108, 500
Note that the 1st two have leading zero's. The specs are that we don't want these displayed. However, we do want zero's which aren't leading displayed, i.e. the 2nd zero in 050, and the middle zero in 108, as well as the last two zero's in 500.

In order accomplish this, you will need to design logic to figure out if the zero is leading or not. If it is, the logic should activate the blanking input on the associated driver which will blank out the leading zero.

WARNING: THIS IS ONE OF THE ITEMS WHICH I WILL FAIL YOU ON IF I THINK YOU HAVE TAKEN THE EASY WAY OUT AND BLOWN IT OFF.

SPECS - BOTTOM of board

I must be able to see the wire wrap to grade it and I don’t want to have to unscrew anything to get at it! The bottom spec is that it needs to be plexiglass mounted on 1 inch standoffs. However, the pictorial shows some other ideas if you don't want to use plexiglass.

SPECS - NOISE

The required accuracy is 1% of 808 inches: I run the project up a hallway for 808 inches. This accuracy req’t is for me. Sometimes I don’t run a perfectly straight line which adds some distance to the course. Design your project as accurate as you can.

Once I go forward 808 inches, I go backwards to starting line. Hope it says 0 at the end! Note I said 0, not 000.
This test course has a problem with it. The entire course is under very electrically noisy lighting and it goes by three different electrically noisy labs. Your wire-wrap rats nests will pick up this noise big time! I'm constantly seeing projects that do one of several things.
They might just go blank all of a sudden, (could also be due to a short)
Or the jump ahead or backwards in the count huge or small amounts.
or they freeze up.
any idea how to fix this noise problem?
Capacitors
Right. Where should they be placed
<Bledsoe, John> Between VCC and Gnd

<Jones, Richard> where on board?

<Prichett, James> On the socket.

<Bledsoe, John> Close to chip

<Jones, Richard> Right. As close to Vcc and ground on the chip as possible. The size should be fairly small so you don't slow the chip down. When you buy wire wrap sockets, buy them at least one size larger then you need. Use the extra holes in the socket to put your capacitor on.

<Jones, Richard> There should also be a larger cap at the power inputs to the board. This one should be electrolytic and make sure it is in the correct polarity.

<Jones, Richard> There is a pictorial document that you should download. You don't have to print it but look at it with acrobat to observe some ideas. We will look at it next week.

**SPECS - Board Protection**

<Jones, Richard> While we are talking about the input to the board, wise students protect their boards from reverse polarity supplies. I have heard many a SOB story about every chip blowing on the last day. All I can say is that it was an expensive lesson since I won't give more time on the project. Protection diodes are CHEAP. The course and grade are not!

**SPECS - “+ -” sign**

<Jones, Richard> Plus sign for going forward, minus when going backwards. Remember that D - FF we talked about earlier?

**PROJECT WIRE-WRAP**

<Wilson, Dick> How many wraps on a post can we have?

<Jones, Richard> We will talk wire wrap next week, but it depends on what kind of wire wrap sockets you buy. Most students buy the 3 wrap sockets.

<Bledsoe, John> Do they make a wire wrap socket big enough for the LCD?

<Jones, Richard> No they don't but if you look at the pictorial document, there are several choices shown on how to accomplish this. One is that they make some inline wire wrap strips that are 40 pins long. Just cut one in half and put it in at the correct separation. Another is to get a 20 pin socket and cut it in half length wise so that you can spread it out.

<Jones, Richard> The pictorial shows several ways to hold the sockets into to the sire-wrap board. One way is to use the socket wrap id's which also have pin numbers on them. The hole for pin #1 is smaller then the rest and it holds the sockets in great.

<Jones, Richard> The other way is the Poor Mans id which is nothing more than covering the bottom with masking tape. You can write the pin numbers on the tape when you push the socket thru. This idea works as long as you are gentle.
The hold gets loose after a time.

<Prichett, James> Will the standard cap leads/other discrete components stay in the wire wrap socket without solder?

<Jones, Richard> It will be a very tight fit. You might even need a knife to shave the leads down a bit. Note that you will be needing either a 555 or a 556 for the backplane. Most people use a 555 but put it in a much larger socket so they can put the two C's and R's in with it. See the pictorial for an example.

**PROJECT FORMAL REPORT**

<Jones, Richard> Formal report required. Read the Formal Report format documents on the homepage. Delete the CHIP level schematic req't on page 4 of the project specs. More later.

**PROJECT FORMAL REPORT COST ESTIMATE**

<Jones, Richard> Note the req't for a cost estimate to me for the prototype. Do not amortize the cost over many units. I am only buying ONE! I expect a prototype to COST! Don't forget, you have a company to run. You have overhead. Just a few items is labor, social security, benefits, rent, electric, insurance, etc....