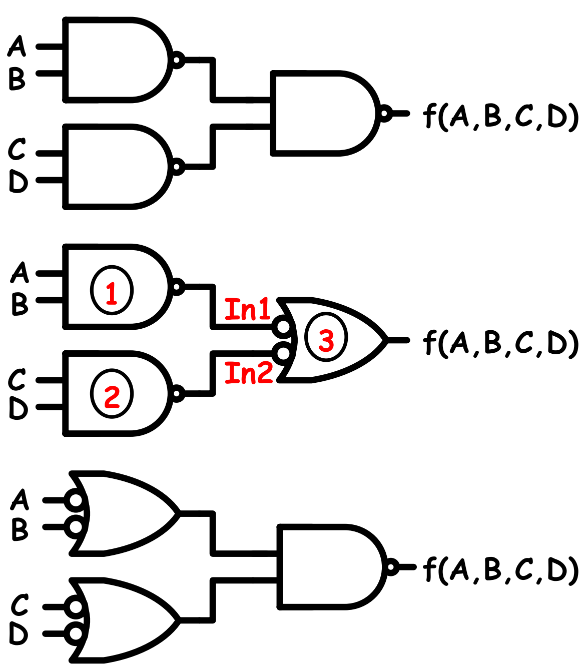
Combinational Logic (C)

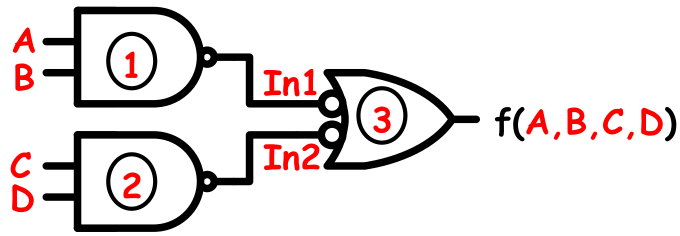
Now that we have learned about the ***Positive*** and ***Negative logic*** systems of thought, what do we do with it? **Why bother with Negative logic at all**? There are several reasons for using one or the other and there are times when they both should be used in a Combinational Logic Circuit. We will look at this first.

The figure below has 3 circuits which are all **equivalent to each other**. The top one is what you are used to seeing, consisting totally of ***Positive logic***. In order to analyze this circuit, one must apply all possible signals to the four inputs to determine the output. The result will be the table to the right.

A	B	C	D	f(A,B,C,D)
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1



Let's evaluate the 2nd circuit:



- Gate 3 will be **HIGH** when **at least one** input is **LOW**.
- Input #1 will be **LOW** when **both** inputs of gate 1 are **HIGH**.
- Input #2 will be **LOW** when **both** inputs of gate 2 are **HIGH**.
- So, we get a **HIGH** output for the conditions:

$$\underbrace{0011}_{3} \quad \underbrace{0111}_{7} \quad \underbrace{1011}_{11} \quad \underbrace{1100}_{12} \quad \underbrace{1101}_{13} \quad \underbrace{1110}_{14} \quad \underbrace{1111}_{15}$$

Matching the Bubbles

However, that's the hard way of looking at it. Note that the bubbles are matched up on this circuit. Anytime you can match up inversion bubbles, you can ignore them in the analysis (ie. they cancel each other out). Now we can take a second look at the circuit but this time we will take into account the matched bubbles and cancel them out.

Gate 3's output **will achieve its active state (HIGH), when either;**

BOTH A and B are HIGH **OR** BOTH C and D are HIGH.

This logic will result in the same list of min-terms as before. This list has been written in a more concise form below called a **Switching expression** which we will discuss later.

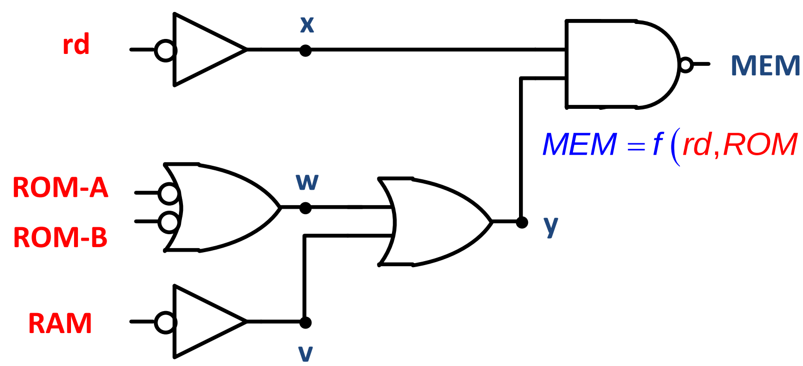
$$f(A,B,C,D) = \sum m(3,7,11,12,13,14,15)$$

Q: So, when would you use **circuit 1** or **3**?

A: Well, quite often, the way a circuit's inputs and outputs are represented is determined by what kind of logic level is the desired end result level for some action to take place. The third circuit is an **Active Low** circuit which is looking for Low inputs and will provide an **Active Low** output to some device which **needs a low to complete some specific action**. The next example is one such circuit which follows those rules.

***Positive / Negative Logic Example*:**

Problem Statement: The circuit below generates a logical **ACTIVE LOW** output, "**MEM**", which is then used to activate memory IC's in a microcomputer. Determine the **min-term set** which will activate "**MEM**".



$MEM = f(rd, ROM-A, ROM-B, RAM)$

- MEM is an ACTIVE-LOW output. So, **both** x **&** y must equal 1 for MEM = 0.
  - x = 1 when rd = 0.
  - y = 1 when **either** w **or** v = 1.
    - v = 1 when RAM = 0.
    - w = 1 when **either** ROM-A **OR** ROM-B = 0.
- So, MEM = 0 **only** when rd= 0 **and at least** 1 of ROM - A, ROM-B, or RAM = 0.

$MEM(rd, ROM-A, ROM-B, RAM) = \sum m(7, 8, 9 \ldots 15)$
$= \prod M(0, 1, 2, 3, 4, 5, 6)$