Design considerations (D)

In order to properly design a system, the designer must consider other items than just the 'logic' of the circuit. We will discuss:

- **Power Consumption**
- **Propagation delays**
- * **Gate fan-in and fan-out restrictions**

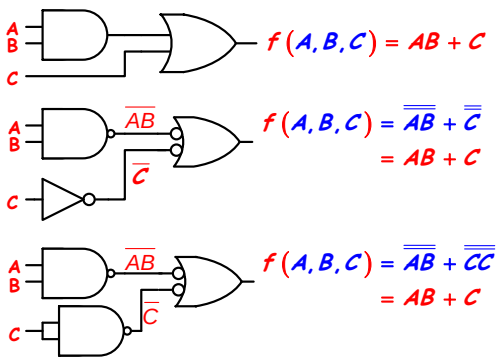
Unused gate Inputs

Question: If we have to choose, what type of basic gates do you use?

Answer: **NAND gate**

- **Cheaper**
- **Draws less current**

Question: What to do with those pesky extra, unused inputs!



Note that in the bottom circuit to the right that a **NAND gate with its inputs shorted** together has been substituted for a **NOT gate**.

Question: Why was this done?

Let's look at the truth table for a **2-input NAND** gate:

A	B	OUT
0	0	1
0	1	1
1	0	1
1	1	0

Assume that **input A** in the truth table to the right is the unused input. If we were to **tie it to ground (the top 2 rows)**, the output would always be **HIGH**. On the other hand, if we were to **tie the input A to V_{cc} (the bottom 2 rows)**, the output could vary depending on the level of **Input B**. Therefore, one choice for the unused inputs would be to tie them to V_{cc}. A second choice would be to tie all the inputs together with the used inputs.

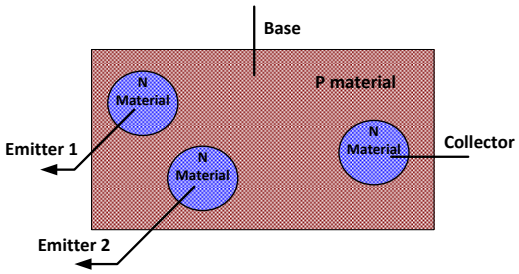
Unused Input Current Usage

We now have a NAND gate with an unused input and we have to choose between 2 choices:

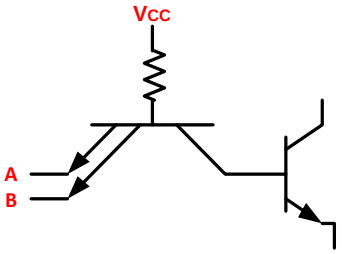
- **Short the inputs together, or**
- **Tie the unused input to V_{cc}.**

Which one of these choices I choose **depends on the current usage which will result**. In order to understand that it is necessary to go back to the beginning of the design of the gate itself on the substrate level.

First, look at a substrate level representation of the transistor on the input stage of a **NAND gate** is built. The nice thing about a **NAND gate** is that whenever the fabricator needs an extra input on a gate, he just dopes in a little extra **N material** on the **P material substrate**.



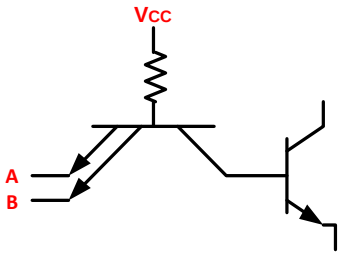
The figure above has **two emitters**. If an additional one were to be needed in the chip fabrication process, another section would be doped with some more **N type material**. This would add in another emitter. Note that this only works in the digital world. It is not as straight forward in linear usages of transistors.



The circuit above represents the input stage of a **NAND gate**.

Question: Consider our two choices based on **power consumption alone. Would one method use more power than the other?**

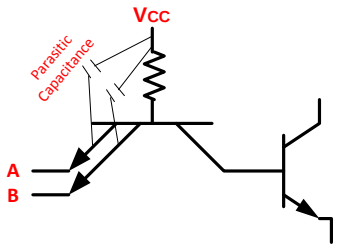
Answer Analysis:



- When both inputs are being used (or shorted together), the current from the single base is split between the two emitters. So, everything else being equal, the current would be split between the two inputs.
- When one of the inputs is tied to V_{cc}, the same amount of current is being drawn from the base.

Answer: Therefore, there is **no power advantage to either of the two choices based on power.**

Let's continue our examination of what happens if we were to **tie the unused input to V_{cc}** instead of shorting the two inputs together. The figure to the right is the same input stage as before but this time **some parasitic capacitances between each emitter and the base have been added in**.



Question: Is this parasitic capacitance a problem?

Answer analysis

As stated earlier, one use for the unused inputs would be to **tie the excess inputs** on the **NAND gate** to V_{cc} and **send the signal to be inverted through a single input.** The problem with this lies in the parasitic capacitances. Tying the input to V_{cc} would cause some unnecessary parasitic noise to be asserted onto V_{cc} bus. This would then increase the need to filter the bus.

Answer: **So, if the designer has a choice, he shouldn't tie the NAND extra inputs to V_{cc}!**

Unused NOR gate inputs

Question: What do we do with the unused inputs on an OR gate?

A	B	NOR
0	0	1
0	1	0
1	0	0
1	1	0

Answer Analysis:

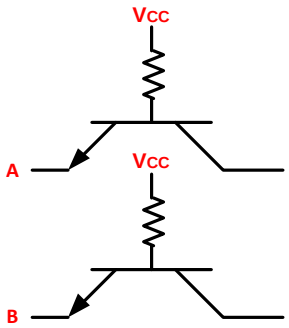
Examine the **NOR gate** table to the right.

- It can be seen that if the unused input, **A**, were to be tied to V_{cc}, (bottom 2 rows), the output would be permanently **LOW**, while
- if it were tied to **ground** (top 2 rows) the output could vary based on input **B**.

Answer: Therefore, based on logic, **one choice would be to tie the unused inputs to ground. Naturally, the other choice would be to short the inputs together.**

Question: **How about current usage?**

Answer Analysis



The figure to the right is the **input stage** for a **NOR gate**.

Again, if you examine the choices based on **power consumption**, this time you will note that if input **A** were grounded, the gate **would only use half the current (thus half the power)** than it would use if both **"Base to Emitter"** junctions were on. The current here is **additive**, so **if you can reduce the number of inputs which are used, you can save on power**.

Answer: For **NOR** gates, **tie unused inputs to ground. Don't short them together.**

AND / OR gate extra inputs

Question: What do you do with the extra inputs on **AND** gates and **OR** gates?

Answer: The answer to this question is based on the input stages of the devices.

- **AND** gates have the same input stage as **NAND** gates, therefore, **we would use the NAND gate results on extra inputs.**
- **OR** gates have the same input stage as **NOR** gates, therefore we would **use the NOR gate results on extra inputs.**

Delay times

In an ideal world, everything would happen instantaneously. A pulse placed on the input of a gate would result in a perfectly shaped result on the output with zero time delay. But in the real world, the laws of physics take precedence and the **voltage parameter can't change instantaneously or perfectly**.

Why does it happen? The gate isn't just a black box. The internal circuitry has response time restrictions which causes problems. The transistor switches have speed problems which cause rising and falling edges of the output waveforms to be sloped instead of vertical. The specifications which cover this characteristic are known as **RISE** and **FALL times.** Along with this time problem is the fact that it takes time for the effect of the **input change** is felt at the output. This is **"Propagation delay."** These characteristics are the basic limitation which controls how fast the system responds. It takes time for the signal to have its effect cascaded through all the devices which make up the gate. **The more complex the internal circuitry, the slower the response time.**

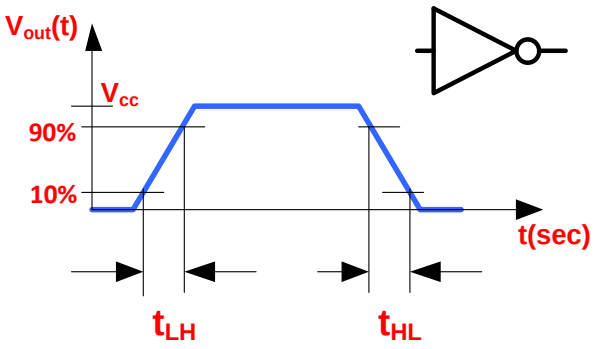
Rise and Fall time

Two very important characteristics of a gate are the times that the output takes to change due to a change of the input. The time it takes the **OUTPUT** to go from **Low-High (t_{LH}) & High-Low (t_{HL})** are seldom the same, so they require different nomenclature:

- t_{LH} ⇨ **delay,** output goes **Low** to **High**
- t_{HL} ⇨ **delay,** output goes **High** to **Low**

By convention, these measurements are taken at **10%** and **90%** of **peak values**. With these two values, you can determine the maximum switching frequency:

$$f_{max} = \frac{1}{t_{LH} + t_{HL}} (hz)$$



The equation indicates that the smaller the denominator, the higher the frequency.

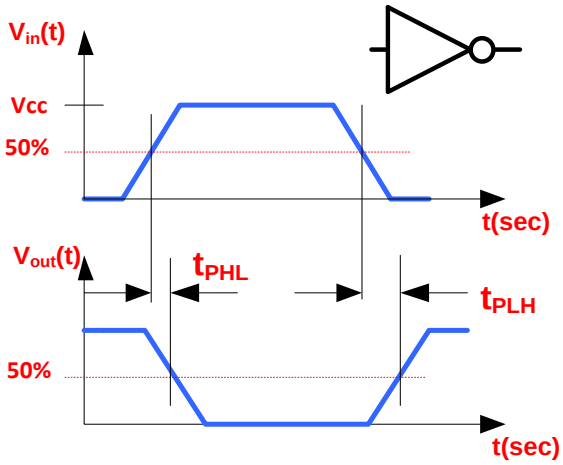
Propagation Delay

The delay between signal in & output change is called: **Propagation delay**. It is a **function** of:

- **gate complexity**
- **temperature**
- **voltage**
- **fan-out / in**

The **Propagation Delay** value is used to determine the **physical delay of a logic signal as it propagates through a series of gates.**

Propagation delay is measured at two different time intervals. The first interval, t_{pHL}, is the delay for an **output transition from High to Low**, while t_{pLH}, is the delay for an **output transition from Low to High.** As can be seen in the waveforms below, the measurements are taken at **the 50% of peak value points.**



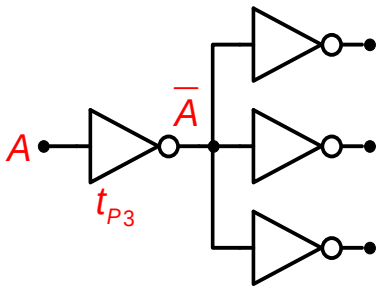
Sometimes these values aren't available as separate values. When that is the case, the designer can find a value for propagation delay which is an average of the two values.

$$t_{pD} = \frac{t_{pLH} + t_{pHL}}{2}$$

The effect of Fan-out and Fan-in on Propagation delay

Effect of Fan-out

A gate's switching speed depends **on the number of inputs which are driven by the output of the gate**. Generally, **increasing the fan-out slows down the logic flow** through the gate. The circuit to the right has a single inverter driving three other inputs.



The **total propagation time** for the 1st gate would be the no-load propagation time of the inverter + the propagation times of each of the gates attached to it. So, the **propagation time** of the gate to drive the load would be:

$$t_{p3} = t_{p0} + 3t_{pL}$$

Effect of Fan-in

The **fan-in** of the device also affects the propagation time. In general, the **larger the number of inputs a gate has, the slower the device is**. This is due to the fact that the more inputs devices have the more complex the internal circuitry is which can slow down the switching response.

The following two tables demonstrate nominal values for t_{pD}, t_{PHL} & t_{PLH} for different families and gates.[1]

Propagation Delays of Primative 74LS series gates[1]

	Propagation Delay	Power Dissipation	
Logic Family	tPD	per Gate (mW)	Technology
7400	10	10	Standard TTL
74S00	3	19	Schottky TTL
74LS00	9.5	2	Low-Power Schottky
74ALS00	3.5	1.3	Advanced LS
74HC00	8	0.17	High Speed CMOS

Power Dissipation & Propagation delays for some Logic Families[1]

		t_{PLH}		t_{PHL}	
Chip	Function	Typ.	Max.	Typ.	Max.
74LS04	NOT	9	15	10	15
74LS00	NAND	9	15	10	15
74LS02	NOR	10	15	10	15
74LS08	AND	8	15	10	20
74LS32	OR	14	22	14	22

[1] The TTL DATA BOOK, Volume 2, Texas Instruments, Inc, Dallas, Tx., 1985