History of Semi-Custom Logic Devices

5.0 Introduction

Over the years, the number of gates on a single chip have grown from a few gates on the 7400 series to over 1 million in a **VLSI (Very Large Scale Integration)** chip. As a general rule, the higher the integration, the lower the PCB (Printed Circuit Board) costs and the lower the power requirements for the board.

Digital logic can be implemented on several levels:

Name	Complexity	Gates per Chip
SSI	Small Scale Integration	Fewer than 12
MSI	Medium Scale Integration	12 to 99
LSI	Large Scale Integration	100 to 9999
VLSI	Very Large Scale Integration	10,000 to 99,999 (CUSTOMIZED)
ULSI	Ultra Large-Scale Integration	100,000 to 999,999
GSI	Giga-Scale Integration	1,000,000 or more

There are also Semi-Customized VLSI devices.

SSI, MSI, & LSI are very nice since they are **off the shelf**, but the chip count, thus the cost can easily get out of control. It's more **cost-effective** to use **custom** and **semi-custom** chips to reduce the cost of projects which will **result in large numbers of units.**

5.1 The Programmable Logic Device

One type of semi-customizable device is the **gate-array**. The 1st phase is to build a chip (at the factory) with a large number of unconnected gates. Later, when the user supplies his needs, the connections are **fabricated into it at the factory.**

5.2 Field Programmable Logic Device (FPLD)

The process of sending your needs to the factory leaves a lot to be desired. In addition, it adds unnecessary costs and time delays to the project. The fabrication of the connections can be placed in the **users hands** by connecting all the gates in the 1st step with flexible interconnection layers. **These connections can be modified electrically by the user.** The FPLD is developed by 1st designing the logic expressions, translating them into the PLD format, then using a **PLD Programmer to program the array** by removing the unwanted connections.

5.3 Logic Arrays

Programmable Logic Arrays are built around homogeneous arrays of elements which can make up **OR & AND gates**. One way to make these gates is with a series of diodes and demonstrated in the diode review.