## 5.5.3 PROGRAMMABLE ARRAY LOGIC (PAL).

When the OR-array is pre-programed (fixed) and the AND-array is programmable, you have what is known as a PAL/GAL. These are very low cost replacements for discrete gates. The PAL was developed to overcome certain disadvantages of the PLA such as longer delays due to the additional fusible links that result from using two programmable arrays and more circuit complexity. The PAL is the most common one-time programmable logic device. A PAL which <u>can be re-programmed</u> is known as a GAL, Generic Array Logic. Besides being re-programmable, the GAL also differs from the PAL by normally having programmable output configurations. The GAL is re-programmable because it uses E<sup>2</sup>CMOS (electrically erasable CMOS) technology instead of bipolar technology and fusible links which is the normal PAL technology.

The PAL/GAL is often used for look-up tables where speed is important. It's faster to look up the answer than it is to calculate it. Unlike the PROM in which all  $2^n$  possible products of 'n' variables are generated, a PAL/GAL generates a limited # of product terms. Therefore, the cost is less than for PROM's and FPLA's. They are available in packages with essentially the same technologies as the PROM. Essentially, what this means is that each output OR has a locked in number of product terms available to it.



## 5.6 Device availability

All of these devices are chosen based on the # of inputs, the # of outputs, and the output polarity. (See the table below.) If one of the product terms in a OR array doesn't get used, <u>leave all of the links in</u> <u>place</u>. Since any literal AND'd with its inverse will equal '0', it will not affect the circuit. Since you will save programming time by not burning links unnecessarily, it will be to your benefit.

Device	Name	Inputs	Product Terms	Outputs	Output Polarity	
PAL18P8	PAL	18	8	8	Programable	
PAL16L8	PAL	16	8	8	Active Low	
PAL16L8 => PAL with 16 inputs, Active-Low output, and 8 outputs						
PAL16C1	PAL	16	16	1	Complementary	
PAL14H4	PAL	14	4	4	Active High	
GAL16V8	GAL	16	??	8	Variable	
GAL16V8 => GAL with 16 inputs, Variable output configuration, 8 outputs						
PLS100	PLA	16	48	8	Programable	
PLS153	PLA	16	42	10	Programable	
825123	PROM	5	32	8	Active High	
825129	PROM	8	256	4	Active High	
825131	PROM	9	512	4	Active High	
825135	PROM	8	256	8	Active High	
825137	PROM	10	1024	4	Active High	
825147	PROM	9	512	8	Active High	
825181	PROM	10	1024	8	Active High	
825185	PROM	11	2048	4	Active High	
825191	PROM	11	2048	8	Active High	
825321	PROM	12	4096	8	Active High	

## Some typical commercial PLD's

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## 5.8 GAL Output Logic Macrocells

- 1. GALs contain OLMCs (Output Logic Macrocells).
- 2. OLMCs in the GAL16V8 contain programmable logic circuits that can be configured in three basic modes
  - Simple
    - In this mode, the OLMCs are configured as dedicated active combinational outputs or as dedicated inputs (limited to six).
    - $\circ$  The three possible configurations in the simple mode are:
      - Combinational output
      - Combinational output with feedback to an AND array
      - Dedicated input
    - In this mode, the OLMC can produce up to eight product terms in an SOP expression.
  - Complex
    - $\circ$  In this mode, the OLMCs can be configured two ways:
      - Combinational output
      - Combinational input/output (I/O)
    - The OLMC can produce up to seven product terms in an SOP expression.
  - Registered
    - $\circ$  In this mode, the OLMCs can be configured two ways:
      - Registered
      - Combinational input/output (I/O)
    - In the registered mode, a D flip-flop in each OLMC synchronizes all registered output data to a common clock edge.
    - The registered outputs have up to eight product terms in an SOP.

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5.8.1	OLMC Configurations	
	Combinational output	
	AND arrays OR array Output Polarity	
	Control Input	
	Combinational output with Feedback to AND arrays	
	AND arrays OR array	



