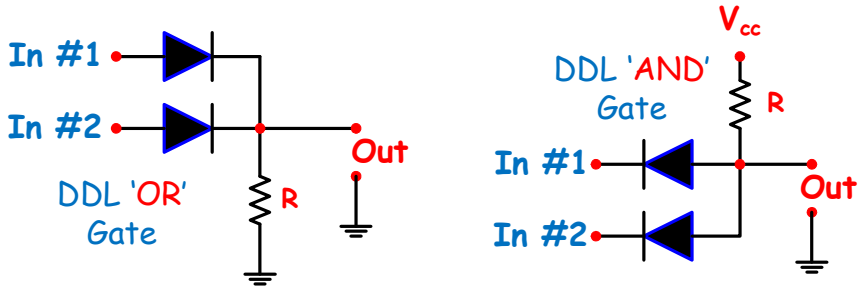
A1.1(a) Diode-to-Diode Logic (DDL)

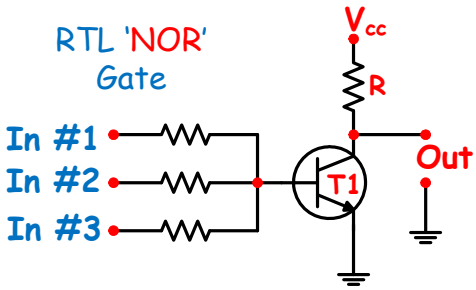
DDL was the 1st attempt at a logic family.



DDL is **VERY fast** but limited in the type of gates since it lacks inversion ability.
(If you don't understand the purpose of the **Pull-Down** and **Pull-Up** resistors, then skip ahead to their discussion)

A1.1(b) Resistor-to-Transistor Logic (RTL)

Designers next tried to design using the capabilities of transistors. The **NOR Gate** to the right demonstrates how this could work. By placing several transistors together, you can have "**NAND's**", "**NOR's**", "**AND's**", "**OR's**", "**NOT's**", etc.



If any input is high, the voltage on the base of T1 is enough to saturate T1.

With a single input you now have a NOT gate. We now have fixed the issue of a limited number of gates.

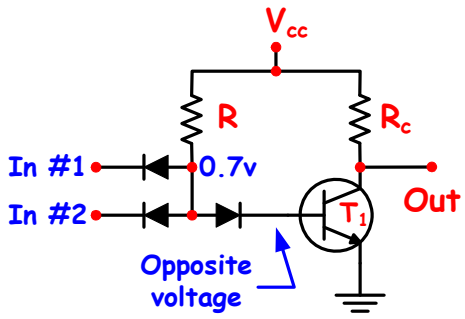
In #1	*In #2*	*In #3*	*Output*
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Disadvantages of RTL are:

- Saturation means **speed loss**,
- **High Power dissipation** due to the large R and high collector current.

A1.1(c) Diode-to-Transistor Logic (DTL)

If either input is grounded, (0), T_1 is off, and the output will be high, (1).



In #1	In #2	Output
0	0	1
0	1	1
1	0	1
1	1	0

Problems with DTL

When T1 is saturated, it is **HEAVILY SATURATED**! So it runs **hot** and it takes a **LONG** time to become unsaturated! Thus, you have a **MAJOR speed loss**. (It takes time to clear electrons from the base regions)

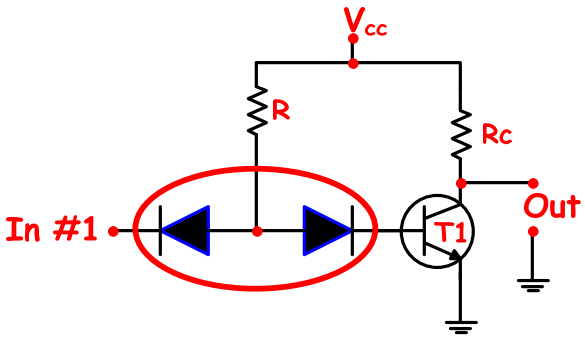
Therefore, both **DTL** and **RTL** are **VERY SLOW** and **VERY POWER** inefficient.

Section A1.1 Review Questions:

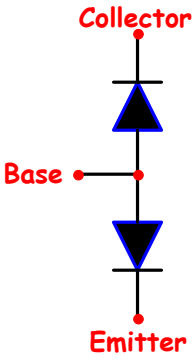
1. What are the primary technology advancement (advantage) of **DDL**?
2. What is the major disadvantage of **DDL**?
3. What is the major advantage of **RTL** over **DDL**?
4. What are the major disadvantages of **RTL** and **DTL**?

A1.2(a) Transition to a better design: TTL Development

So far all attempts at a valid semiconductor logic design have been found lacking. However, it was soon noticed that there was a relationship between transistors and the diodes at the input of a **DTL** device. Observe the **DTL inverter** below.

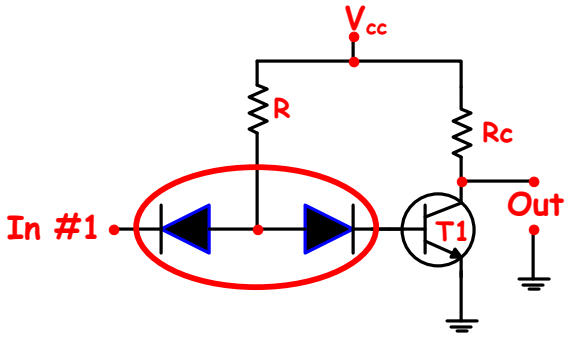


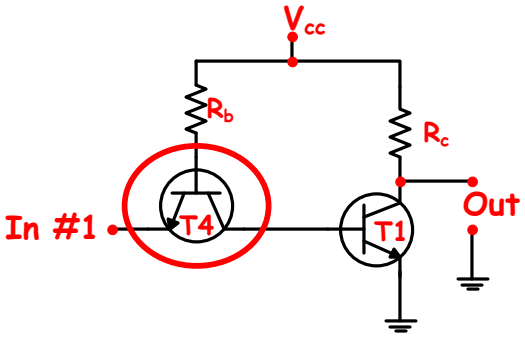
In #1	Output
0	1
1	0



If you focus on the relationship between the two diodes (circled), you should note that they resemble the model of a transistor introduced during your devices introduction course.

Remember that you can model a transistor with two back-to-back diodes as shown to the left. Note that the input configuration of the DTL inverter looks just like this. So, why not replace the two diodes with a transistor as shown below?

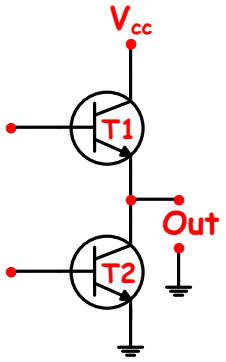




You now have an early generation **TTL inverter** or **NOT** gate! This early NOT gate had **POWER dissipation** problems due to the size of R_C.

A1.2(b) The Totem Pole Output Stage

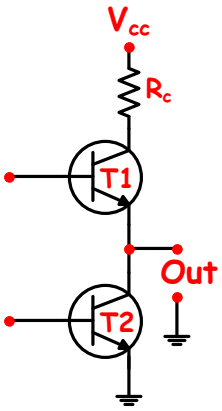
To help to solve this power dissipation problem, the early designers returned to another circuit which was introduced in the intro devices course, the **Push-Pull** or **Totem Pole** circuit, shown to the lower right.



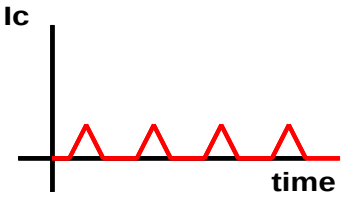
Ideally, there is no time in which both **T1** and **T2** are ON at the same time. For this reason there is a **relatively small amount of collector current.**

A **High (1)** and a **Low (0)** can still be obtained on the output but the reduction in collector current causes a **significant drop in power dissipation**.

But now there is a new problem. By removing R_C you have **removed protection from T1**. If the output is shorted to ground while **T1** is on, I_C **skyrockets and T1 blows up!!!**



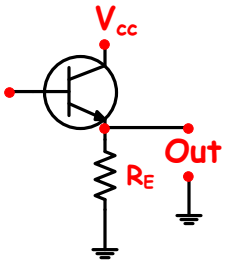
So, a small collector resistor is added back into the circuit (on the order of 330 ohms. The collector current looks something like:



A1.2(c) Driving the Totem Pole

The addition of the **Totem Pole output stage** now requires a method of driving the two bases. The problem is that they must be driven in such a way that **when one is on the other is off**. So, let's again go back to the **Intro to Devices** course and remember two very important transistor configurations.

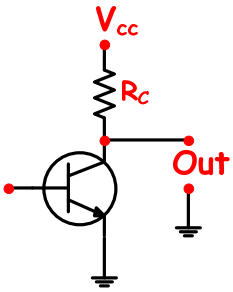
The Common-Collector Configuration



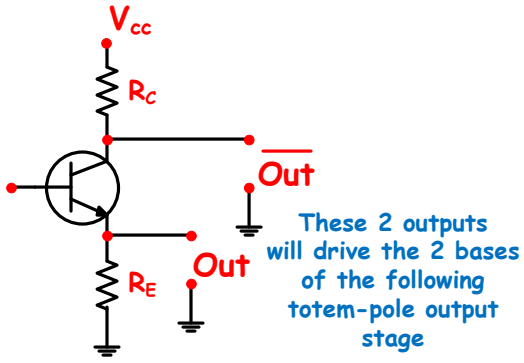
The 1st configuration is the **Common Collector configuration (also known as the Emitter Follower)** shown to the left. In this configuration, **the output is in phase with the input**.

The Common-Emitter Configuration

The second configuration of interest is the **Common-Emitter circuit.** In this circuit there is a **180 degree phase shift between the input and the output.**



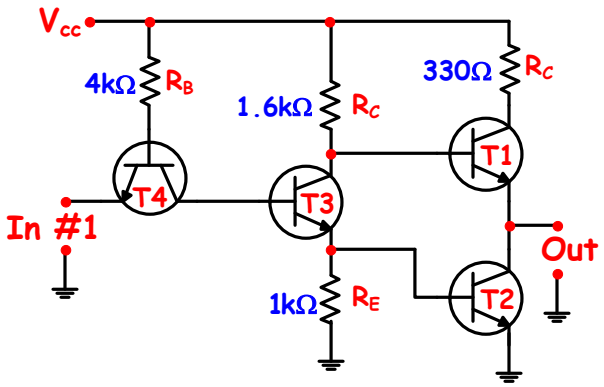
The Phase-Splitter



If we combine these two circuits into a single transistor circuit we get the '**Phase Splitter**'. The relatively high R_C keeps the collector current low so **power dissipation will remain low**.

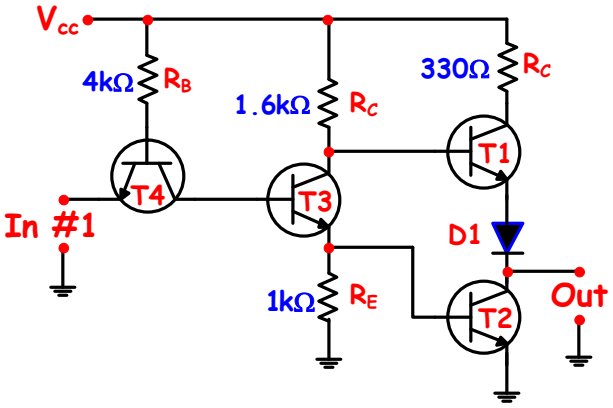
Now we have two outputs which are **180 degrees out of phase with each other** to drive the bases of the totem pole output.

A1.2(d) Putting it all together for a basic TTL circuit



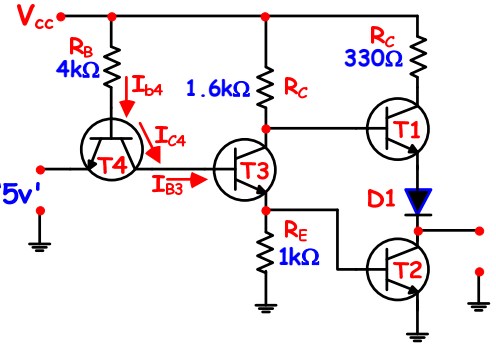
We now have a good attempt at a basic TTL inverter. But there still is a problem. There are still times when both **T1** and **T2** are **on at the same time due to biasing issues**.

We can fix this by adding a diode (shown) so that it now takes (0.7v + 0.7 v = 1.4v) across the Base to Emitter junction to turn T_1 on.

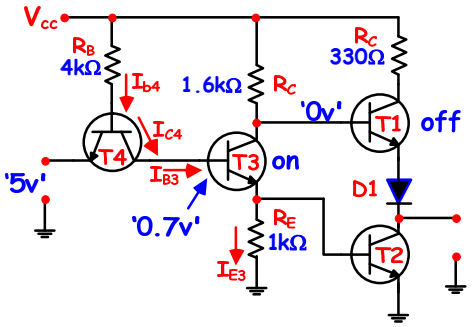


A1.2(e) Example for a HIGH (1) input

Let's now put everything together into one big circuit with some voltages applied.

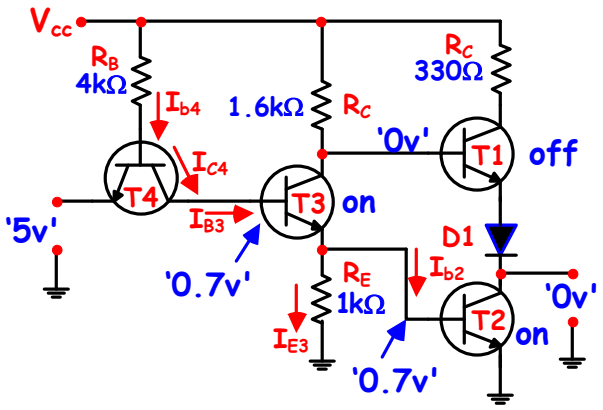


When a '**logic 1**' is placed on the input **T4** is still acting like two diodes, not a transistor. **T4** passes base current thru to the collector which supplies base current to **T3**.



The current on the base of **T3** turns **T3** on. The V_{BE} of **T3** will be **0.7V**. Since **T3** is on, **T1** will be **biased off**.

Note that T3 and T2 act like a Darlington Pair in that when one is ON the other will be OFF. V_{BE2} will be 0.7v which turns T2 ON and the output voltage will be a logic 0 (0v), as you would expect in an Inverter.



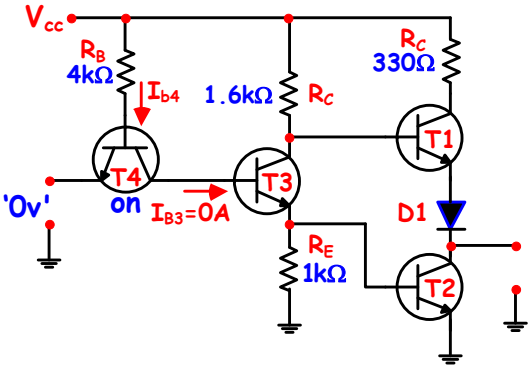
We still have a problem which is difficult to solve.

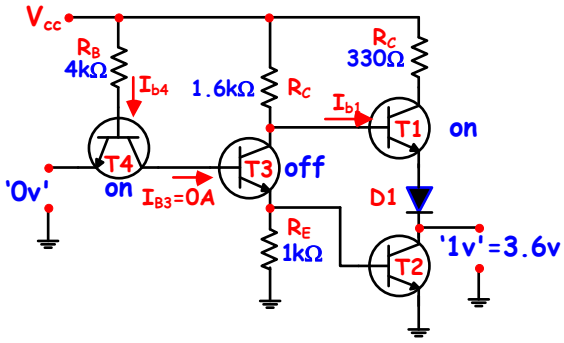
QUESTION: What happens if **T2** is **ON** and the output gets shorted to V_{CC}?

ANSWER: **T2** is now directly connected to V_{CC} without **T1** or R_C around to protect it. Can you say "**Vaporization**"???? We will have to live with this problem.

A1.2(f) **Example with a LOW (0) input**

With a '**logic 0**' on **T4**'s emitter, **T4** is **OFF** and there is **no collector current** feeding into **T3**'s base.



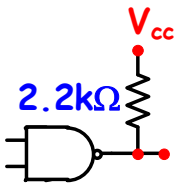


Since there is 0A on I_{B3}, **T3** is **OFF**. This turns **T1** **ON** and **T2** **OFF**. Since **T2** is **OFF**, there will be a '**Logic 1**' on the output.

Note that the **logic 1** is **NOT 5v**. In this slide it is **3.6v** but it can go as low as **2.4v**.

- The low **logic 1** issue is one of the **MAJOR PROBLEMS** with **TTL**. The Texas Instruments **TTL NAND** gate (**7400**) has a **logic 1** swing all the way down to **2.4v**.
  - When connected to the inputs of other devices inputs it is necessary to hold the input emitters in a reverse bias condition. Therefore, **2.4v is enough**. Also, for this same reason, all it has to do is provide for leakage currents.

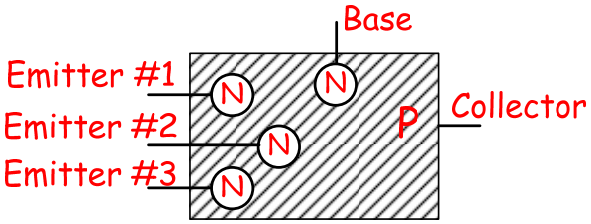
- If it is necessary to have a true **logic 1** output then use a **pull-up resistor** connected to V_{CC} to '**PULL**' the output up to **5v**.

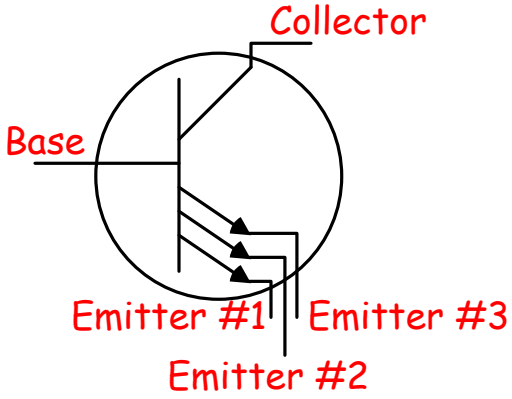


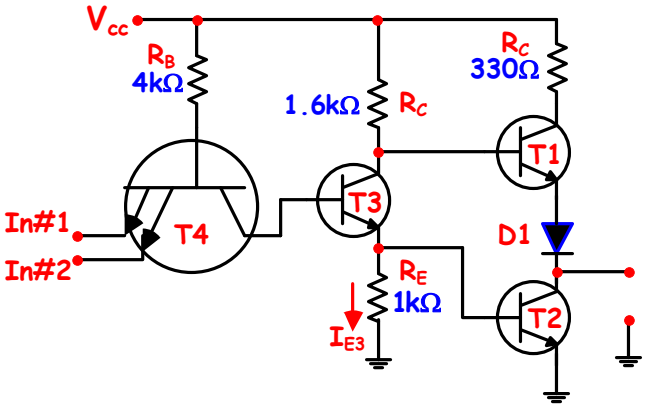
One place where this is necessary is when connecting the output of a TTL logic family to the input of another logic family such as **CMOS**.

A1.2(g) **Adding inputs**

If the fabricator needs more inputs, all they do is **dope** in additional **N material** inside the large **P material** area.







The circuit shown above right is a two input NAND gate. If any or all inputs are at a logic 0 the base current will be shorted to ground. The only way for **T4** to be ON is if both inputs are at a **logic 1**.

IMPORTANT!

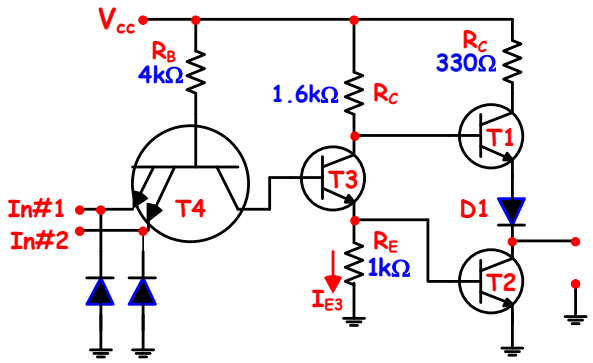
Note that if any input is left **floating**, **T4** will interpret it as a logic 1. This is not as bad as it is with CMOS but it still is not a good idea.

QUESTION: Why is it not a good idea?

ANSWER: The main reason is because **floating inputs are susceptible to noise and ringing**. **Good engineering practice is to not allow floating inputs**.

So, as a general rule, you should never leave any INPUT unconnected. If the input is not used, you connect it to one of several things depending on LOGIC or POWER usage. You can connect to another input, in effect shorting them together. You can also connect them to ground, or to V_{cc}. Care must be taken to insure that whatever you connect them to, you have not changed the logic of the gate.

The circuit to the right has two diodes added to inputs to provide **high frequency noise immunity**.



We now have a class of logic gates which is fast, and relatively noise free.

A1.3 TTL Advantages

- The **phase splitter** doesn't saturate due to R_E. **T1** will saturate but it won't because of careful biasing. **T4** won't saturate and it isn't acting as a transistor anyway. This leaves us with **T3** which does still have some issues if driven hard which we will talk about later.
- We are left with a device which can be driven **VERY hard**. The standard **TTL** family can be driven as hard as **20Mhz**. Some **TTL** families we will discuss can be driven up **90MHZ**.
- GENERAL RULE: The **FASTER** you drive a device, the larger the amount of **CURRENT YOU DRAW** and the **LARGER THE AMOUNT OF POWER YOU DISSIPATE!**

Sections A1.2 and A1.3 Review questions:

1. **(T/F)** The TTL input transistor acts like a transistor.
2. The removal of the collector resistor from the totem pole output causes a danger of what?
3. The output of the emitter follower is **(in / out of)** phase with the input.
4. The output of the common emitter is **(in / out of)** phase with the input.
5. The purpose of the **Phase Splitter** is to drive the bases of the **totem pole** output stage in such a way that_____.
6. The purpose of **D1** is to _____.
7. **TTL** floating inputs are interpreted as logic _____.
8. The major danger of floating inputs is _____.
9. **Standard** TTL can be driven as fast as _____hz.
10. As a general rule, the **faster (harder)** that you drive a **TTL** device, the more _____ and the more _____.

A1.4 TTL Family Numbering and Identification

- TTL families and subfamilies are indentified by the prefix of **74** for **commercial devices** and by a **54** for **military devices**. The prime difference is that military devices have been tested to much more stringent specifications. The additional strict testing increases the cost of the devices by a significant amount. In some devices, the actual design of the device has been modified but the devices are still pin-to-pin compatible with like numbered devices from the opposite category.
- After the prefix comes the **family ID letters**. If the device is a standard TTL there will not be any letters following the prefix. All other subfamilies will have a set of letters to identify it.
- Following the subfamily ID is a set of numbers (either two or three digits) identifying the actual device type.
    - For the remaining lecture, I will use either two (XX) or three (XXX) x's as place holders for these numbers.
- There may be letter or two after the ID number to identify the packaging of the device.
    - So, if a device is labeled as a **54LS00**, you have a **military grade**, **Low Power Schottky**, **NAND** gate.
    - A **7400** is a standard **TTL NAND** gate.

A1.5 TTL Subfamilies, Part 1

The standard TTL design has had several different changes made to it to achieve different characteristics. The first three are shown below

Standard TTL	**74xx**	**Runs at a max speed of 35MHz**
High Speed TTL	**74Hxx**	**Achieved by lowering resistor values. Being replaced by Schottky TTL (discussed later)**
Low Power TTL	**74Lxx**	**Slowest of the TTL family. Achieved by raising resistor values. Speed is slower because I_C is lower. Being challenged by CMOS.**

Section A1.4 and A1.5 Review Questions

1. Military Grade **TTL** devices have a _____ prefix.
2. A **7400** is a _____.
3. A **54L08** is a _____.
4. A **54H04** is a _____.
5. The slowest of the **TTL** family is _____.

A1.6 Understanding the Totem Pole Output Stage

Understanding the **Totem Pole** output stage is fairly important when designing with **TTL**.

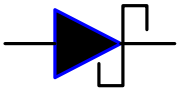
- One of the main trouble spots is the period of time when **T1** and **T2** are swapping states.
- During this period both **transistors conduct HEAVILY**. The instantaneous current is about **10 times the normal level of supply current.**
- This is good because it **speeds up the switching time.**
- However, it also pulls a huge current spike out of the power supply **(up to 30-40 mA). This spike lasts up to 10ns.**
- Unless a good **de-spiking capacitor** is used (**Mounted as close to the chip as possible** between V_{cc} and ground), this could cause a lot of **noise issues** with other IC's in the system. There could also be significant corruption of the V_{cc} bus extending the noise to the entire system.

A1.7 More of Current Spiking

A second problem with current spiking is that TTL does not perform well in wiring environments known as "**rat's nests**". This is just the type of environment that one would see in a wire-wrap board.

- De-spiking capacitors (mentioned above) should be placed as close to each chip as possible (between V_{cc} and **Ground**) and perhaps salted though out the board as well.
- Use a short lead ceramic or **tantalum** capacitor **(.01 to .1 microfarad)** mounted between V_{CC} and **Ground** **as close to each chip** as possible.
- In addition, place a **10 microfarad, 6V tantalum capacitor** between V_{CC} and **Ground** where the supply enters the circuit board.

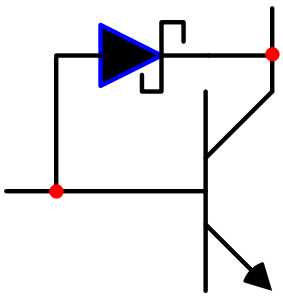
A1.8(a) The Schottky Diode



- Another device you should remember from your devices course is the **Schottky Diode**.
- It was created **because the 74Hxx series was not fast enough**. The **Schottky** is a '**metalized' diode** with a V_f = **0.2v**
- Of course, you can get a V_f **of 0.2v** with a germanium diode as well, but **germanium diodes can't handle the high currents that a Schottky can.**

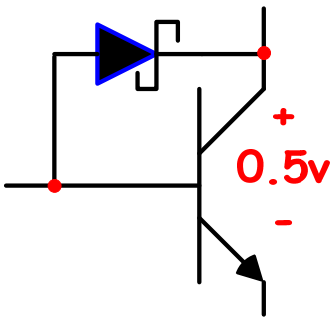
A1.8(b) The Schottky Transistor

- In order to keep the **transistor switching speed as high as possible**, it is important to keep its V_{CE} > 0V.
- If this is **done, the transistor will stay out of saturation.**
- **We accomplish this by taking a regular transistor and placing a Schottky Diode between the Base and the Collector as shown in the circuit to the right.**



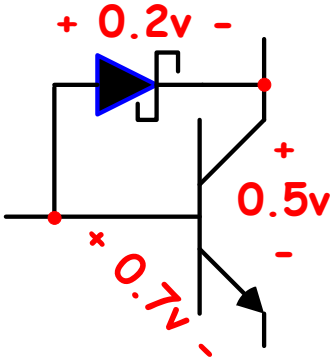
- **It is usually assumed V_{BE} = 0.7V for a transistor which is on.**
- **This is not true. It is actually a bit lower than that.**

- Let's assume that V_{CE} =0.5v as a transistor turns on.



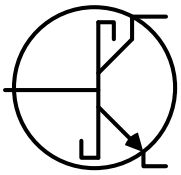
- If V_{CE} =0.5v as a transistor turns on, KVL says that once the V_{BE} junction reaches V_{BE} =0.7v, the excess current will shunt thru the Schottky diode.

$$V_f + V_{CE} = V_{BE}$$
$$0.2v + 0.5v = 0.7v$$



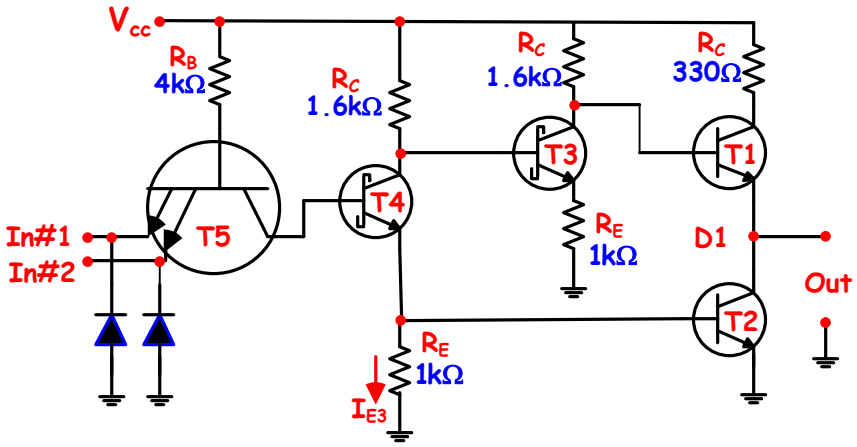
- This keeps the transistor well out of saturation so we can now drive it VERY HARD and it will not saturate due to the low V_F rating of the Schottky diode.
- This creates a situation where we can build VERY fast gates.
- The T_{PHL} and T_{PLH} of a 74S00 NAND gate is 3ns compared to the 22ns max rating for T_{PLH} and 15ns max for T_{PHL} of a 7400.
- Of course, there is some cost to the increased speed capability. The Low Level Output Current (IOL) is on the order of 20mA compared to 16mA for the 7400. BIG DEAL!

With the addition of the Schottky diode, we now have a new type of transistor: The Schottky Transistor



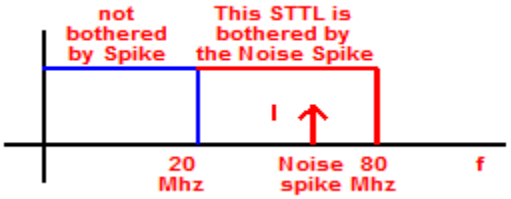
A1.8(c) The Schottky Gate

We can now create a vastly improved gate by making a few modifications to the TTL internal circuitry.



We now have the **74S00 (a Schottky NAND gate)**. Note that the addition of **T3** above **eliminated the need for a biasing diode**.

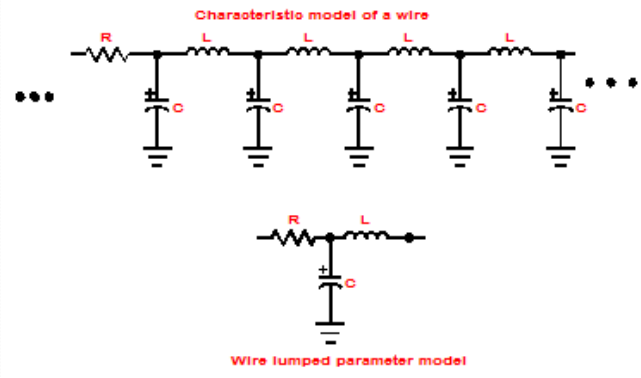
- **Schottky gates run at speeds up twice (80Mhz) that of the standard TTL gate.**
- **They run a bit hotter than normal gates so they need special layout care.**
- **The wider bandwidth causes more noise to make it into the data stream.**



Schottky and Noise Review Questions:

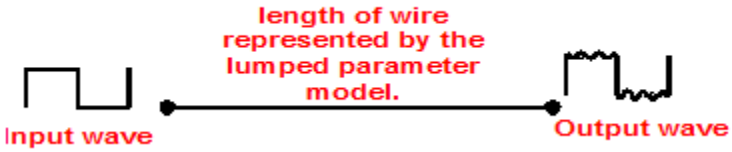
UNDER CONSTRUCTION********

In order to limit the effect of noise, we need to keep wire lengths as short as possible. We can take a wire and build a model of it which looks like the following:



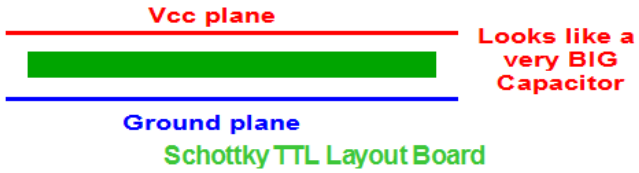
The lumped model looks just like a Low pass π filter. Below is what the equivalent filter created by the wire will do to a square wave.

What happened? The output square-wave has had all the high freq's chopped off by the effective low-pass filter of the wire. Therefore, the sharp edges of the input waveform are gone. Remember that the Fourier expansion for a square wave is the odd harmonics of freq. (EET 305)



It's not just the wires which are important. V_{cc} and **Gnd** act like very long wires. One way to fight this problem in applications where noise is something which is definitely not desired is the Schottky TTL Layout Board.

This board has a solid copper ground plane on one side and a solid copper Vcc plane on the other. It has pre-drilled holes for components which are isolated from either plane. If it is desired to attach V_{cc} or **Ground**, a solder connection is made. The two planes with the non-conductive center is illustrated below.



It makes the entire board look like a VERY CLEAN Power Supply

There is another reason to keep wire lengths short. Wire Propagation delays are approximately 1ns/1ft of wire.

LS TTL

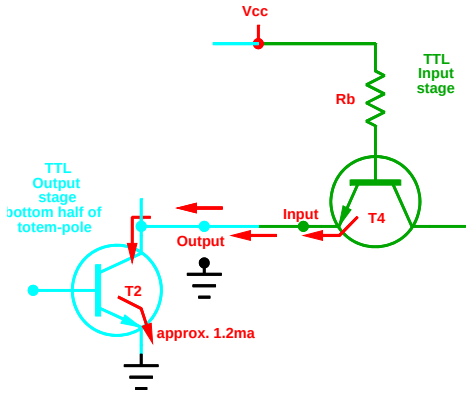
Q: Why not take the STTL chip and raise the resistor values like we did before to lower power usage?

A: We do. The STTL series resistor values are raised. The Power dissipation goes down significantly, but it slows the chip down from 80Mhz to around 40Mhz. This is still faster than regular TTL and it dissipates much less power.

74LSXX Series

Interconnecting TTL

When connecting TTL devices, you have to consider load conditions. The lower transistor of the totem-pole output stage of a basic TTL Chip is designed such that the collector I_c can be up to 12 ma. So, it can **sink** 12 ma when ON.



Q: How many 1.2ma loads can you drive with your one TTL output?

A: 10*1.2ma=12ma

So, you can drive 10 loads. This is where the infamous "Fanout" of 10 comes from.

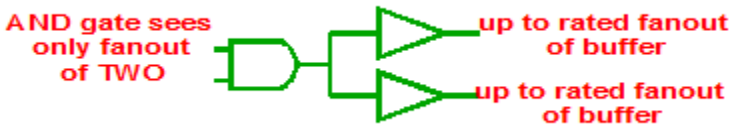
Standard TTL fanout is 10. (when driving devices from the same TTL subfamily.

LSTTL Fanout is 20 when driven by Standard TTL.

Each device is guaranteed to run at rated speed at worst case currents for the designed fanout.

Q: What do you do if you want to drive more than 10 loads with one TTL output?

A: Put a buffer in the middle.



Regular TTL	will drive	10 regular TTL inputs 20 LS TTL inputs
Low-Power TTL	will drive	2 regular TTL inputs 5 LS TTL inputs
High-Power TTL	will drive	12 regular TTL inputs 40 LS TTL inputs
Schottky TTL	will drive	12 regular TTL inputs 40 LS TTL inputs
Low-Power Schottky	will drive	5 regular TTL inputs 10 LS TTL inputs

Excerpt from Chart 1-5 of Lancaster's TTL Cookbook

CMOS can drive low power TTL just fine with no major problems. However, if you try to drive a regular TTL, you are limited to a **fanout of '1'**. As noted before, **you can drive CMOS with TTL with the addition of the pull-up resistor**. As usual, in both cases, a careful check of the specs should be made.

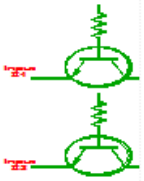
Difference between NAND and NOR front-ends:

Input stage of 2 input NAND and AND gates

Let's look at the difference between NAND and NOR gates.

First, examine the input stage of a standard two input NAND gate. With either input grounded the current out of the pin will be 1.2mA. With both grounded each will output 0.6mA. So **0.6 + 0.6 = 1.2m**. So, if you use a NAND as an inverter by tying the inputs together, the **fanout will be 1**. Note, an AND gate is just a NAND gate with an inverter attached to it so it has the same input stage.

The OR and NOR gate input stages have 2 transistors vice 1. If you tie the two leads together both transistors will be working and the **fanout will be 2**.



Input stage for 2 input NOR and OR gates

If you remember, we discussed what to do with unneeded inputs for ANDs, NANDs, NOR's, and ORs earlier in the semester.

Finally we need to discuss how we might connect TTL devices to a bus. There are two main ways which have been built into different types of TTL chips.

Open Collector Outputs

A gate with an **Open-collector output** is a gate which can only pull its output down to zero. If the output voltage is supposed to be '1', the connection is left floating. Therefore, the output would not be able to drive any device which requires a '1' like an LED. The reason for this type of device is to allow more than one output to use an input pin (bus). It can easily be seen, that if one device were to have a '0' output and another had a '1' output that there would be a conflict. This conflict can cause high currents and destruction of the gate. In order to make the output change from a float to a 1, a pull-up resistor should go to V_{cc} to 'pull' the output up to a logic '1'. The resistor is chosen to be large enough (usually around 1k to 2.2k ohms) that it can be easily overcome by the pull-down resistors of any attached gates. This system is fairly limited. As many open collector outputs can be connected to a pull-up resistor as you want. But the only time that the output will be pulled high is when none of the outputs are pulling down on the resistor. For this reason, **Open Collector** type devices are not very popular.

Tri-state Outputs

To overcome the problems of the **Open-collector** type devices such as **limited speed**, **poor noise immunity**, and **limited usefulness**, the **Tri-state logic** was invented. It has been the solution to sharing a single bus line with many outputs of other devices. A third state other than a logic 0 or a logic 1 is added. This state is the **High Z** or **HIGH IMPEDANCE** state. In this state, the internal circuitry is essentially disconnected from the output. Only when the order is applied to cause the **High Z** state to go away can a 0 or a 1 be asserted onto an output line. Tri-state devices have a third wire to which the command to switch to and from **High Z** is sent. There are special devices called data selectors which is the TTL version of a one-way switch (which we have discussed) which have been developed to act as traffic cops for this type of system.

REVIEW QUESTIONS

UNDER CONSTRUCTION