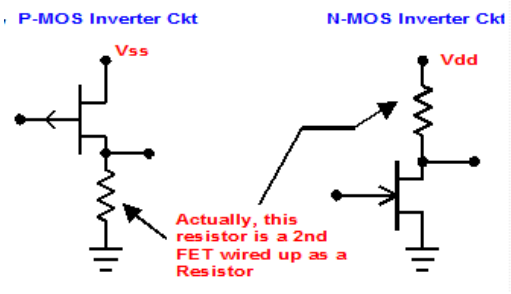
MOS Families:
P-MOS, N-MOS, and CMOS

P-MOS and N-MOS technology was very popular in the early '70's. However, they have been mostly phased out by now. **They have the same problems as RTL, but at a lower current level.**



CMOS Technology

This technology is getting so popular that it is making significant in-roads into TTL territory.

Reason:

- Due to the fact that it uses **N** and **P** channel **MOSFET**'s, the **Input Resistance, R_i, is almost an open circuit**. This means:
- It presents almost **NO FANOUT load on previous gates**. So, Fan-out for **CMOS** is almost unlimited. Data books list **CMOS Fan-out at approximately 100.** But, they also say you can go further. In order to arrive at a Fan-out of 100, they used the worst case leakage current from each transistor combined into **one worst case value**.
- Due to the low Drain/Source Resistance and the high input impedance, Z_i, **power dissipation is next to non-existent.**

History

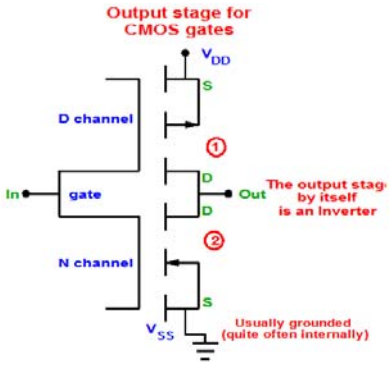
First developed by RCA for **low current logic applications** in the space program. Their name for the technology was:

COSMOS (Complimentary Symmetry MOS)

When the rest of the industry caught on, in order to avoid registered trademark problems, they called the technology **CMOS** which is the official name today. However, **COSMOS** was onboard both Voyager spacecraft (one of which has left the solar system. It worked until Voyager was in the middle of the dust cloud outside of Pluto's orbit.) It was also onboard most of the first moon exploration craft.

How it works:

'0' When a **low (0 volts)** is placed on the GATE, **T1**, will be **OFF** and **T2** will be **ON**, thus producing an output of almost exactly **V_{DD} '1' (5 volts).**



This is a MAJOR **characteristic of CMOS: A 5 volt V_{DD}** will cause a **5 volt HIGH** output. There are very few (and those are almost insignificant) voltage drops. **T2** will be so thoroughly saturated that it will drop **very** low (nv) voltage. In fact, **T2** will be acting like a resistor.

Very clean voltages and low supply current is a CMOS Trademark!

'1' When a **HIGH (5 volts)** is placed the GATE, **T1** is biased **ON** due to the positive voltage on the gate of the N channel. **T2** is biased **OFF** due to the same positive voltage on the gate of the P-channel. **V_{out}** is essentially shorted to ground through **T1**.

MOS transistors are inherently slower than TTL. However, they are more reliable due to fewer semiconductors on the chip to perform the same task, as well as a much lower level of heat development. **CMOS** should be **STONE COLD**.

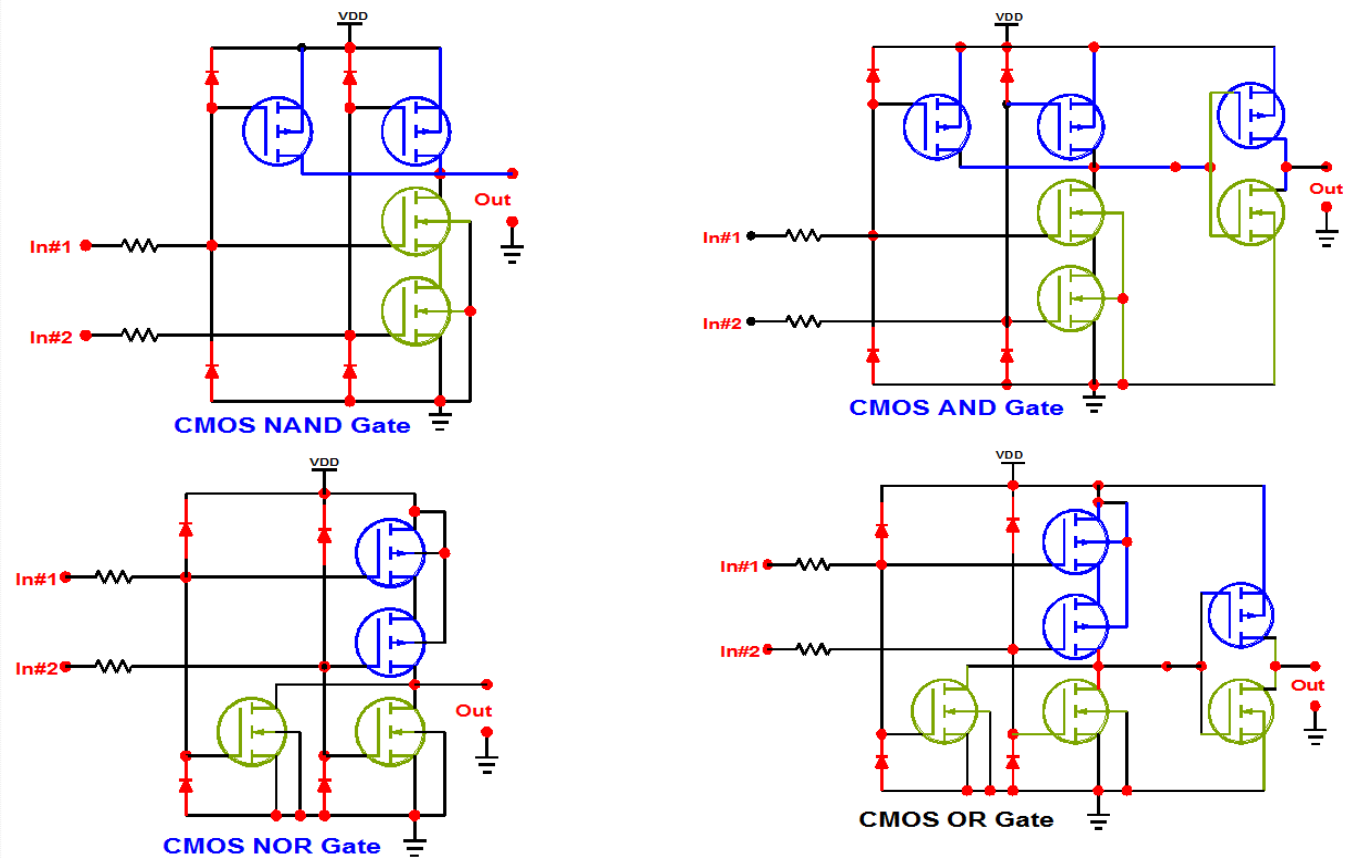
Problem:

CMOS logic does have some inherent problems however.

- It is **VERY** susceptible to **electrostatic damage** due to the high Input Resistance. This makes it **MANDATORY** that you **NOT ALLOW FLOATING inputs. It will destroy the chip!**

When **CMOS** first came out, this was a BIG problem. The gates break down at approximately 80 volts. Static electricity is **MUCH higher** than this! That's not the worst of it. A chip might not show the damage from a jolt immediately! Internal connections may be degraded into a state called "**Latent Failure**". Manufacturers attempt to keep this problem from affecting their chips at their end by:

- Forbidding workers from wearing silk, rayon, nylon, etc.
- Requiring ground straps.
- Making floor and tables out of metal and keeping them grounded every few feet.



A few CMOS subfamilies

- **40xxx** Metal-gate CMOS
- **74Cxxx** Metal-gate, pin-compatible with TTL
- **74HCxxx** Silicon-gate, pin compatible with TTL, high-speed
- **74HCTxxx** Silicon-gate, pin and electrically compatible with TTL, high-speed
- **74ACxxx** Advanced-performance CMOS, not pin or electrically compatible with TTL
- **74ACTxxx** Advanced-performance CMOS, not pin compatible, but electrically compatible with TTL